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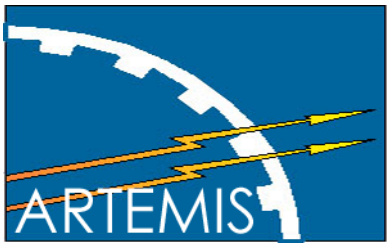

User Guide

Version 6.1

IMAGINATION

TO

REAL-TIME

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Reference Number: RT-LAB User's Guide

Published in Canada

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1 Introduction

1.1 What to Expect from this Guide

This guide explains the ARTEMiS add-on for SimPowerSystems blockset.

1.2 About ARTEMiS

ARTEMiS stands for Avanced Real-Time ElectroMechanical Simulator. It is a plug-in to the SimPowerSystems blockset for Simulink that enables hard real-time simulation of SimPowerSystems models. The objective of 'hard' real-time simulation is that all iteration of the model are completed in a prescribed amount of time at **each** time step.

The 'hard' real-time simulation objective is different that the typical simulation objective. In a normal simulation, one wants the smaller total simulation time or said in another way, the smallest average simulation time step. The 'hard' real-time simulation objective is to have the smaller **maximum** time step.

The second main objective of real-time simulation is to maintain the simulation accuracy to a certain level. This is a potential problem in real-time simulation because it is made with fixed-step solvers. Compared with typical variable-step solvers, the usage of fixed-step solver can lead to innacuracies because there are no built-in accuracy check within the solvers. A typical variable step solver will implicitly compare it results with a higher order algorithm to verify accuracy. With a fixed-step solver, there is no such verification and larger time step always degrade simulation accuracy in some way.

ARTEMiS help reach real-time simulation objectives in several ways. By its characteristics, ARTEMiS can extend the range of time step to achieve both speed and precision for a specific real-time application. In applications where network switching causes numerical oscillations that cannot be damped at time step above minimum hardware limits, ARTEMiS solvers good damping properties successfully damp the spurious oscillations. Furthermore, in applications where some underdamped or high frequency components, relative to the fastest possible sampling time must be taken into account, ARTEMIS improves the precision of those components compared to the trapezoidal or Tustin methods.

Since version 6.0, ARTEMiS offers a new solver called State-Space Nodal which combines the accuracy potential of state-space methods with the natural ability of the nodal approach to handle circuit with a large number of switches. **Consequently, ARTEMiS is no longer limited with regards to the number of coupled switches in a circuit.** which provides some edges in the modelisation of micro-grids or distribution networks to short to use artificial decoupling methods like stublines but also in more standard systems like HVDC or SVC.

In switched power system, ARTEMiS now comes with automatically Inlined Interpolation methods for thyristors and 2-level voltage inverters. These very efficient solver methods detects and compensates for switching events that occur in the middle of time steps. The option works in conjunction with the RT-Events blockset and uses real-time optimized interpolation techniques to improve accuracy.

ARTEMiS provides special model options. It comes with a saturable transformer model based which use flux as state and that does cause algebraic loops. One can also use SimPowerSystems continuous time machine model in conjunction with Simulink higher order fixed-step solvers. In some case, the use of higher order solver can increase notably the precision.

Finally, ARTEMiS comes with specialized models for real-time simulation such as ARTEMiS Distributed Parameter Line and ARTEMiS Stublines that enables distributed simulation of power systems on several CPUs or cores of standard PCs using RT-LAB. The ARTEMiS plug-in is especially designed to work in the RT-LAB real-time environment and shall prove very effective in helping the typical user reach its real-time simulation objectives.

1.3 Intended Audience and Required Skills and Knowledge

The ARTEMIS User Guide is intended for ARTEMiS users. It is recommended that you be familiar with Simulink and SimPowerSystems before getting started.

1.4 Organization of Guide

The followingl guides come with the ARTEMiS documentation:

- Installation Guide
- User Guide

1.5 Conventions

Opal-RT guides use the following conventions:

Table 1: General and Typographical Conventions

THIS CONVENTION	INDICATES
Bold	User interface elements or text that must be typed exactly as shown.
Note:	Emphasizes or supplements parts of the text. You can disregard the information in a note and still complete a task.
Warning:	Describes an action that must be avoided or followed to prevent a loss of data.
Recommendation:	A suggestion that you may or may not follow and still complete a task.
`Code`	Sample code.
Italics	Reference work titles.
Blue Text	Cross-references (internal or external) or hypertext links.

Quick Start

2

This chapter describes how to use the ARTEMiS Add-On to SPS in RT-LAB. For a quick start on how to use the new State-Space Nodal Solver of ARTEMiS, please refer to the 'SSN basics' chapter of this guide.

2.1 Getting Started (Off-line simulation)

To use the ARTEMiS Add-On to SPS:

1. Start MATLAB. Open a Simulink model that uses the blocks from the SimPowerSystems blockset like SPS demo **power_monophaseline**.

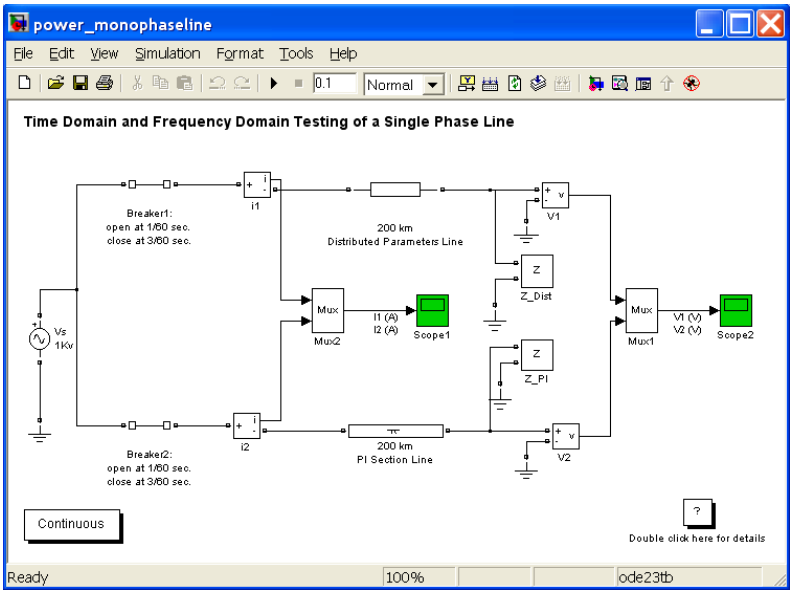


Figure 1:Time Domain and Frequency Domain Testing of Single Phase Line

2. From the MATLAB command window, open the ARTEMiS library prompt by typing **artemis**.

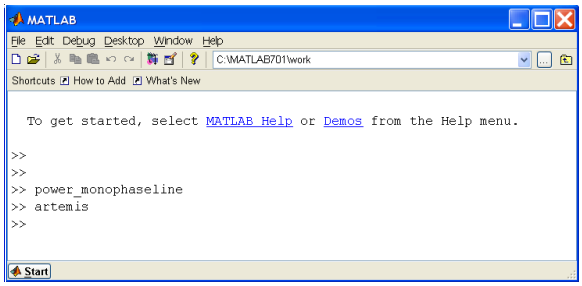


Figure 2:MATLAB

The ARTEMiS library window is displayed.

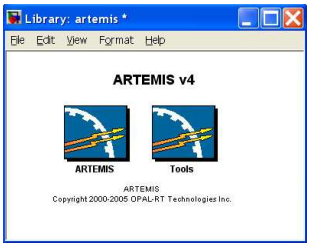


Figure 3:Library ARTEMiS

3. Click on the **ARTEMiS** block and drag the **ARTEMiS Guide** block into your model.

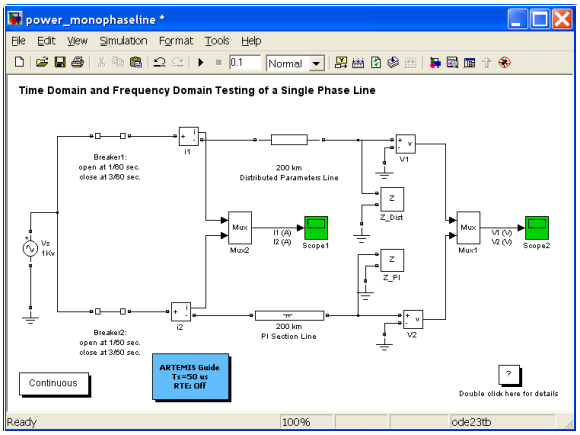


Figure 4:Time Domain and Frequency Domain Testing of Single Phase Line

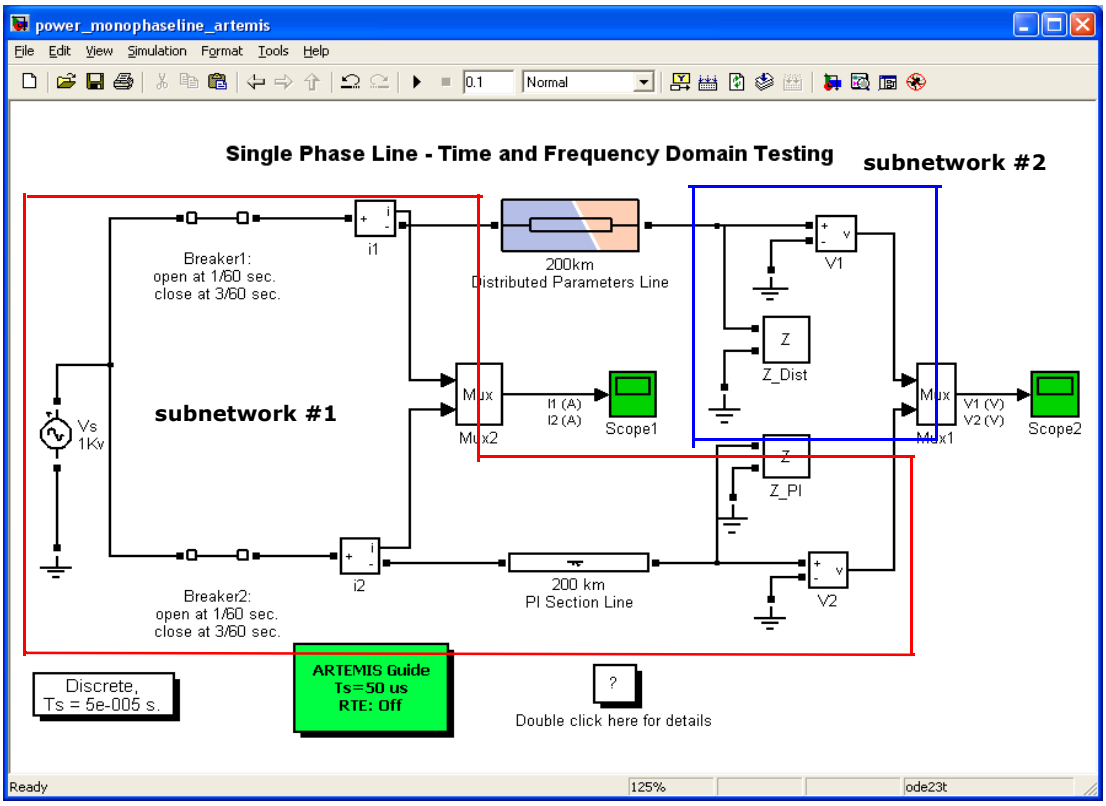
4. Run your model. Once the **ARTEMiS Guide** block is placed in a model, the linear part of power system is simulated using the fixed time step algorithms and options specified in the **ARTEMiS Guide** dialog box. If both the **ARTEMiS Guide** block and the **Discrete System** block from SimPowerSystems blockset are present in a model, the **ARTEMiS Guide** block has precedence.

2.2 Getting Started (RT-LAB real-time simulation)

After the model has run offline successfully, the following step is to modify the model to run it in real-time within RT-LAB.

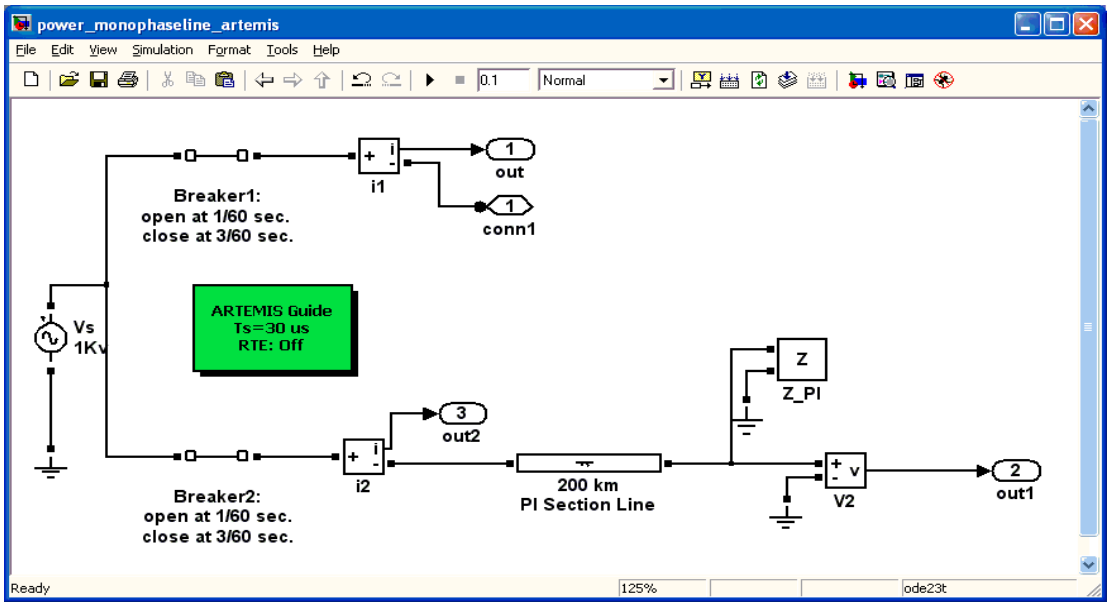
The first step to convert this model to RT-LAB and to exploit the parallel simulation capability of RT-LAB is to convert the SPS Distributed Parameter Line to a ARTEMiS Distributed Parameter Line (DPL). Both DPL models have the same underlying equations but the latter is design to be used inside RT-LAB. The ARTEMiS DPL model can be found in the ARTEMiS library under the ARTEMiS group.

When this DPL model is used, the resulting electric model is effectively decoupled into 2 different state-space systems containing topologically connected elements (RED and BLUE groups of the figure below). RT-LAB will then compute these state-space systems in different cores/CPUs during real-time simulation.

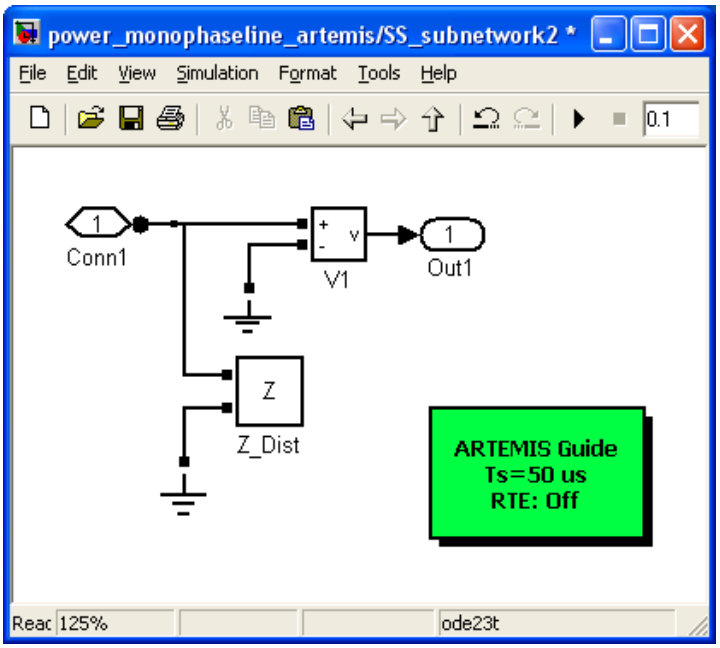


So, step by step:

- Select all blocks located in the subnetwork 1 in the figure above and press Ctrl-G to create a new subsystem.
- Move the ARTEMiS block inside the subsystem.
- Rename this subsystem to SM_Subnetwork_1. The following figure displays the content of the SS_Subnetwork_1 subsystem.

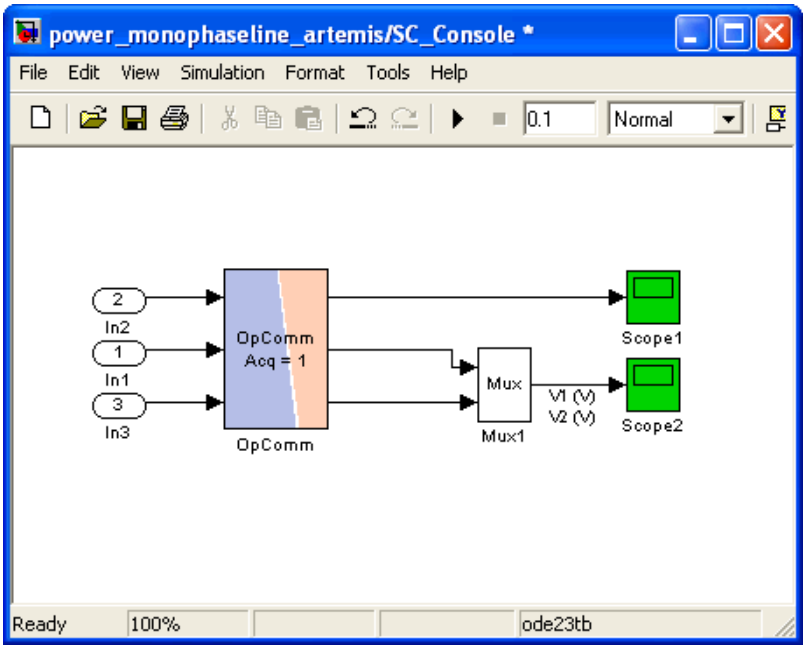


- Select all blocks located in the subnetwork 2 and press Ctrl-G to create a new subsystem.
- Add a ARTEMiS Guide block inside the subsystem.
- Rename this subsystem to SS_Subnetwork_2. The following figure illustrates the content of the SS_Subnetwork_2 subsystem.

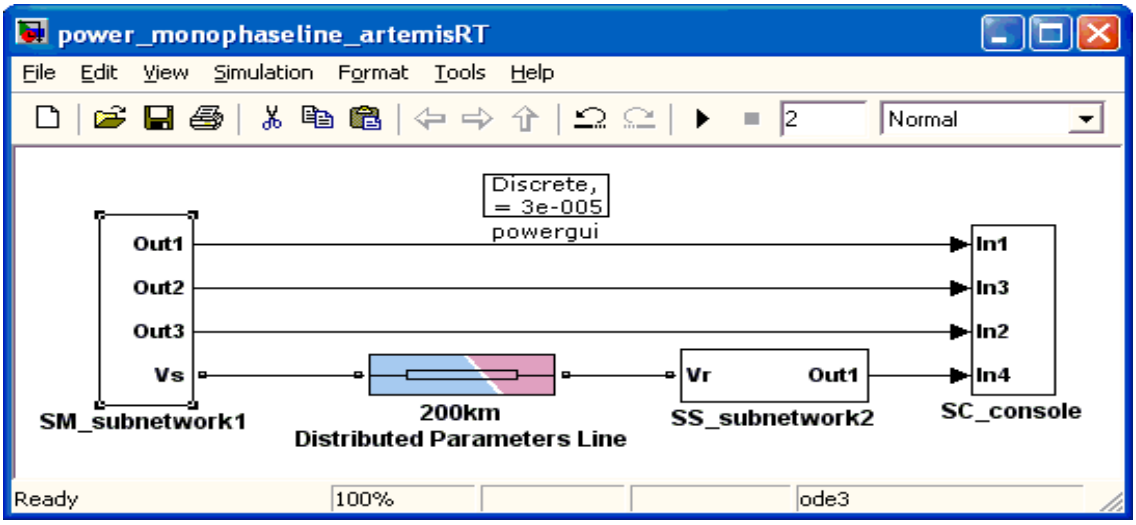


- Select the 3 remaining blocks, normally the two scopes blocks and the Mux1 block and press Ctrl-G to create a new subsystem.
- Rename this subsystem to SC_Console.

- Add the RT-LAB opcomm block between the inports blocks and the content of the subsystem. Don't forget to set the number of inports of the opcomm blocks to 3. Refer to the RT-LAB user guide for more help.
- The following figure illustrates the content of the SC_Console subsystem after the modifications described above have been made.



- Modify the solver parameters of the model; select one of the fixed-step solver, like ode3 for example, and change the fixed-step size to 50e-6.
- Organize the top level blocks according to the following figure. **IMPORTANT: the powerGUI block must be at the top level and each subsystem must contain an ARTEMiS block**



- Save your model.
- Your model is now ready to be compiled with RT-LAB. Refer to the RT-LAB User Guide for more help. If your have set the sample times of your model with a variable set in the workspace(ex: Ts), you should set the model initialization function with <Ts=50e-6;> in File->Model Properties->Callbacks->InitFcn
- IMPORTANT NOTE: A single ARTEMiS block can also be put in the top-level of the RT-LAB ready model. At compilation time, RT-LAB will make a copy of this block with identical parameters in all separated subsystems.

Using ARTEMiS

3

ARTEMiS, the Advanced Real-Time Electro-Mechanical Simulator, is a modular simulation toolset that includes the ARTEMiS Plug-in to the SimPowerSystems blockset.

The ARTEMiS Plug-in is a performance-enhancing add-on product for the SimPowerSystems blockset.

It is easy to use: simply add the ARTEMiS Plug-in block to any Simulink model containing SimPowerSystems blockset blocks and the model runs using the ARTEMiS improved algorithms.

The ARTEMiS Plug-in offers the following advantages to the standard SimPowerSystems Blockset:

- **Real-time computational capability**. More than simply providing faster simulations, ARTEMiS is designed to enable real-time computation of SimPowerSystems blockset circuits. The following considerations were taken into account for the design of ARTEMiS:
  - Precomputation of all state-space matrices due to changing switch topology. This avoids major computational time jitter occurring in the SPS at switching times thus permitting hard real-time simulation.
  - Improved modeling of some power system elements such as: **Saturable transformer** model (which can be simulated at fixed time step in a non-iterative and extrapolation free manner in ARTEMiS)
  - Distributed multi-processors simulation capability of complex power systems with **ARTEMIS Distributed Parameter Line and ARTEMIS stubline** models .
  - Compatibility with OPAL-RT's RT-LAB suite of products for easy integrated parallel simulation design process.
- **Higher precision for linear circuits with high frequency components**: ARTEMiS improves the SimPowerSystems blockset's precision of simulation compared with the standard fixed-step integration methods such as trapezoidal or Tustin, especially for circuits whose variables have high frequency components.
- **Freedom from numerical oscillations without the need for artificial stabilizing snubbers**: ARTEMiS uses stable integration methods that are free from the numerical oscillations that often affect the standard SimPowerSystems blockset fixed-step integration methods such as trapezoidal or Tustin. The effect of ARTEMiS on numerical oscillation can be seen even on simple cases such as SPS demo **power_monophaseline**.

The following section are examples of what can be acheived with the ARTEMIS plug-in to the SimPowerSystems blockset. The Simulink demo section of ARTEMIS contains many more examples.

Since ARTEMiS v6, theState-Space Nodal (SSN) solver is available to simulate in real-time circuit with arbitrarily large number of switches.

3.1 Six Pulse Converter

Because ARTEMiS makes full pre-computation of all state-space equations before the real-time loop, ARTEMiS enables you to gain important computational time when compared to SimPowerSystems.

You can see this using the provided demo **artemis_converterRT.mdl** on RT-LAB. The circuit has 9 states, 16 inputs, 18 outputs and 6 switches. The 3 us gain made with ARTEMiS becomes very important with such tight timing restraints such as PMSM drives with AC-side rectifiers running at 10 us[1].

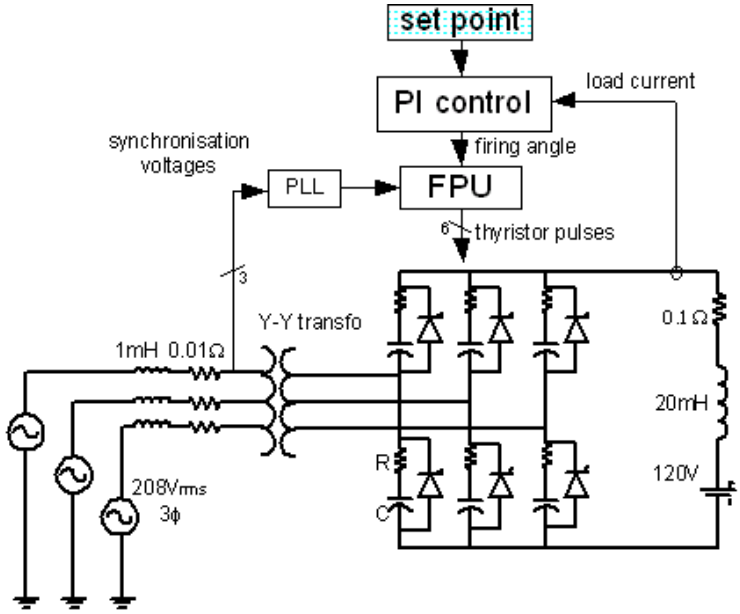


Figure 5:6 Pulse Thyristor Converter and Controller

The next table shows the maximum time step achieved with each solver rather than the average speed. Maximum time step is critical in HIL applications to avoid overruns. The ARTEMiS gain is directly related to the number of switches in the system because SimPowerSystems inverter a nbs-rank matrix, where **nbs** is the number of switches in the network, each time a switch conduction state changes in the simulation.

Table 2: Simulation Step Size for artemis_converterRTL.mdl (Quad-core Opteron, 2.4 GHz, QNX)

PARAMETERS	MAXIMUM CALCULATION TIME (US)
SPS Discrete Solver (Tustin)	13
ARTEMiS, art5	11

3.2 14-Thyristor Frequency Converter

ARTEMiS enables you to gain important computational time when compared to SimPowerSystems because ARTEMiS makes full pre-computation of all state-space equations before the real-time loop.

We demonstrate this in the following frequency converter which is executed on RT-LAB. The circuit has 6 states, 17 inputs, 29 outputs and 14 switches. ARTEMiS is approximately 10 times faster than SimPowerSystems because ARTEMiS pre-computes all state space matrices due to switches before

1.M. Harakawa, H. Yamasaki, T. Nagano, S. Abourida, C. Dufour and J. Bélanger, "Real-Time Simulation of a Complete PMSM Drive at 10 is "Time Step", Proceedings of the 2005 International Power Electronics Conference - Nigata (IPEC-Nigata 2005), April 2005, Nigata, Japan.

entering the real-time loop. This pre-computation requires some memory for storage but a real-time target with 512 Mb of RAM (quite common RAM size for most computers) was sufficient for the test.

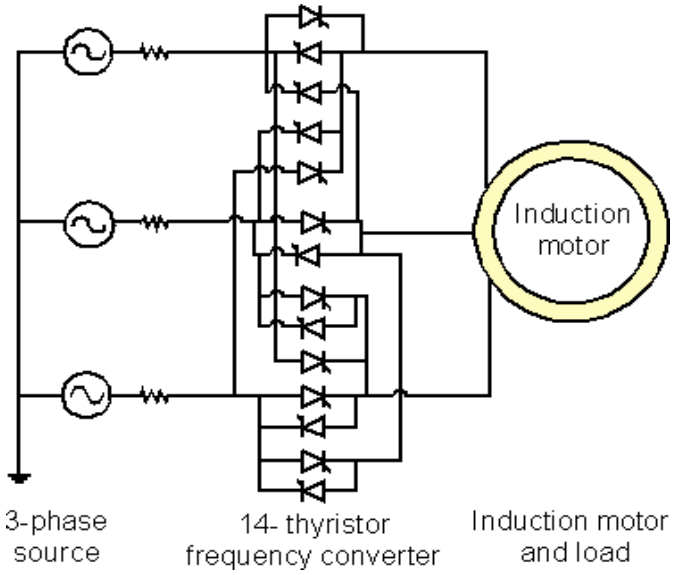


Figure 6:Frequency Converter with 14 Thyristors

The next table shows the maximum time step achieved with each solver rather than the average speed. Maximum time step is critical in HIL applications to avoid overruns. Again, the ARTEMiS gain is directly related to the number of switches in the system because SimPowerSystems inverter a nbs-rank matrix, where **nbs** is the number of switches in the network, each time a switch conduction state changes in the simulation.

Table 3: Calculation Time for 14-Thyristor Frequency Converter (Quad-core Opteron,2.4GHz, QNX)

PARAMETERS	MAXIMUM CALCULATION TIME (US)
SPS Discrete Solver (tustin)	115.0
ARTEMiS, art5	17.5

3.3 Medium Power Network

ARTEMiS comes with specialized models that enable you to gain important computational time when compared to SimPowerSystems. One of those models is the **Distributed Parameter Line** model. In ARTEMiS, the Distributed Parameter Line model is optimized to run in real-time.

The next figure shows a medium-sized power network executed on RT-LAB (**art_power_medium_networkRT**, **art_power_medium_network_multiCPU_RT** demos). The circuit has 5 busses and, most importantly, 9 power lines. ARTEMiS is approximately 10 times faster than SimPowerSystems for this circuit mainly because of the optimized line models. The circuit has only 3 switches which do not hinder the computational performance.

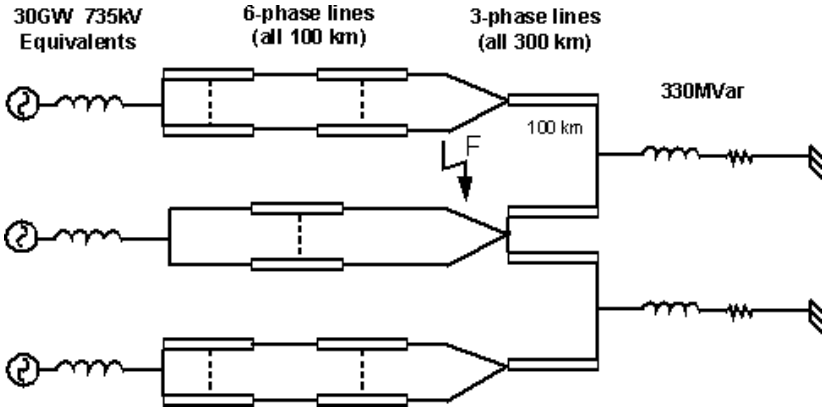


Figure 7:Medium Sized Power Network with 5 Bus and 9 Lines

The table below actually shows the maximum calculation achieved with each solvers and not the average speed. Maximum calculationis the critical factor in HIL applications to avoid overruns.

Table 4: Calculation Time for Medium Sized Network (Quad-core Opteron,2.4GHz, QNX)

PARAMETERS	MAXIMUM CALCULATION TIME (US)
SPS-Tustin Solver, SPS distributed parameter line models	120
ARTEMiS-art5 Solver and ARTEMiS distributed parameter line models 1-core simulation	14
ARTEMiS-art5 Solver and ARTEMiS distributed parameter line models 4-core simulation	9

As can be observed, the speed performance is enhanced by separating the various bus tasks on several core of a the dual quad-core Opteron used in the test. This option is supported by ARTEMiS distributed parameters line models.

3.4 ARTEMiS modeling of transformer saturation

3.4.1 SPS modeling of transformer saturation

The native saturable transformer model of SPS has no linear magnetization branch. The magnetization branch is instead modeled by a current injection. The current injection is computed from a table of the phi=f(i), with the flux being computed from the integral of voltage across magnetization branch.

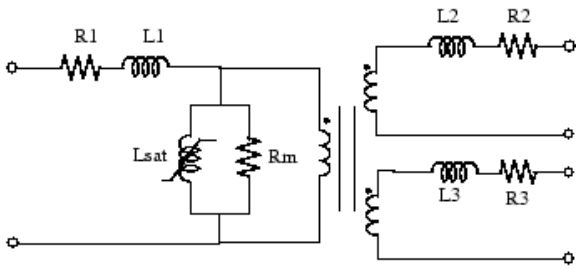
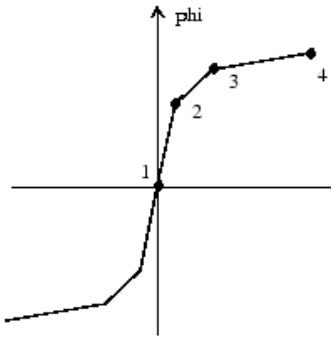


Figure 8:Saturable transformer model in SPS and ARTEMiS

In the SPS model, the non-linear Lsat component of the transformer is completely modeled by a current injection computed from the phi=f(i) characteristics



piecewise segment flux-current characteristic of the magnetization branch of a saturable transformer

In SPS in particular, one can specify a residual flux only when the segment 1-2 has infinite slope as mentioned in the SPS documentation.

3.4.2 ARTEMiS transformer model

In ARTEMiS, a slightly different approach is used that modify the current injection curves by including the linear part of the magnetization curve inside the state space equations describing the system. The modification are as follow:

1-The first segment of the phi=f(i) characteristic is included in the linear part of the state-space system described by ABCD matrices.

2-This linear part is extract from the original phi=f(i) characteristic.

3-The flux across the branch is computed from its linear part phi_linear=L_linear*I_linear

4-A current injection in parallel to the linear inductive branch is used to model the saturation.

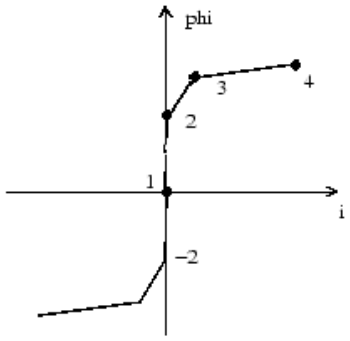


Figure 9:Modified injection characteristic in ARTEMiS caused by the inclusion of the first segment in the linear part of the state-space system

The method can be viewed as follow: in normal mode (non-saturated), the magnetization branch is part of the ABCD state-space system and the branch flux phi is obviously equal to L*i. When saturation occurs, it is like connecting other inductance in parallel to the first one. The important thing to notice is that the voltage across these two inductance is the same, so is the total flux that would be obtain by integration of the voltage across the branch and therefore this flux can be derived from the linear branch and used for current injection.

The differences with SPS native model are the following:

1-The ARTEMiS saturable transformer model requires a non-infinite 1 segment slope to so a state can exist in the ABCD matrices. If not, ARTEMiS will add a very large one.

2-Residual flux can be specified even if the first segment do not has an infinite slope. The implication of this is that the flux will move from the start of the simulation but in a very slow manner because of the very high inductance. The model is therefore adapted to transformer re-energization tests.

3.4.3 Advantages of the approach

The main advantage of the ARTEMiS model is that is can provided accurate fixed-step simulation results without algebraic loops. In SPS, this algebraic loop is caused by the usage of a discrete-integrator (trapezoidal method) in the transformer itself. In ARTEMiS, this flux is computed in the linear part of the state-space system.

SPS provides ways to break this algebraic loop but this can degrade accuracy. See the demo section for more details.

3.4.4 Demos

ARTEMiS provides demos linked to the saturable transformer model.

artemis_power_ctsat.mdl: single phase transformer energization test.

The demo shows an increased accuracy of ARTEMiS over SPS at a time step of 50µs. The flux response of SPS is wrong at 50µs. The ARTEMis response at 50 µs matches correctly the SPS response at 1 µs.

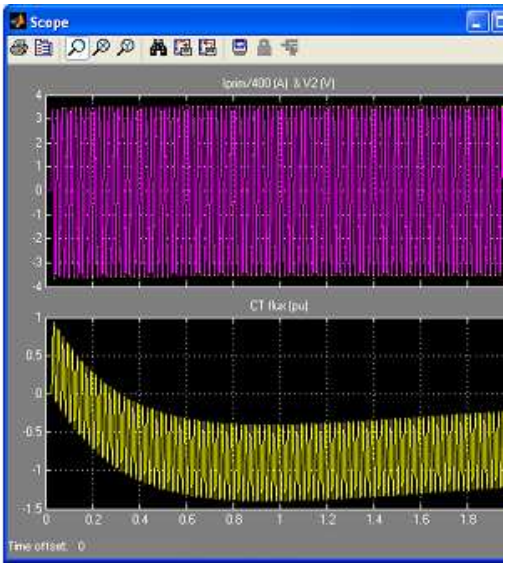


Figure 10:SPS response for artemis_power_ctstat.mdl at 50µs

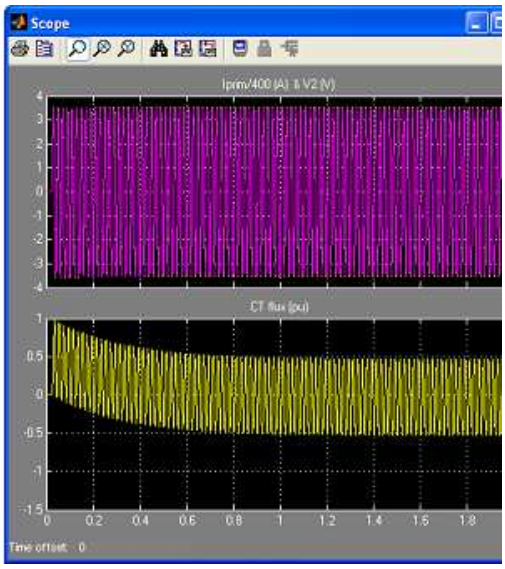


Figure 11:SPS response at 1 µs matching the ARTEMiS response at 50 µs

3.4.5 Initial flux setting

Since ARTEMiS 5.1.4, the initial flux of the transformer can be specified in the transformer mask. In difference with the SPS method, ARTEMiS magnetisation branch is part of the ABCD state-space equation of the simulated system and initial states are set by the state variables.

However, some SPS transformer model don't allow the initialisation of magnetization flux. The following table lists what type of transformer support initial flux setting thought the transformer mask. When not supported, the user must set manually the magnetization inductance initial current in the POWERGUI panel of SPS.

Table 5: List of SimPowerSystems transformer model (R2008 A-B)

Model	Direct Mask initial flux setting support
Saturable transformer	no
Multi-winding transformer	no
Zigzag Phase-Shifting Transformer	no
Three-Phase Transformer (Three Windings)	yes
Three-Phase Transformer (Two Windings)	yes

The ARTEMiS demo untitled: `Fixed-time step simulation of 3 phase saturable transformer without algebraic loop` explains how to compute and set manually the initial flux of a transformer through the Initial States panel of the SPS POWERGUI.

3.4.6 Limitations of the approach

The initial flux should be specified to be within the boundaries of the first segment of the characteristic of the transformer. Numerical instability can occur if it is not the case.

State-Space Space (SSN) solver basics

4

This section explains how to use the SSN solver of ARTEMiS

4.1 Introduction

The State-Space Nodal (SSN) method can be considered as a nodal method. The main difference is how the nodal branch or groups are made. In SSN, the user selects the way the groups are made. These groups are computed by a state-space method while the interface between the groups is solved by a nodal method. By making large groups for example, the number of equivalent nodes to be solved by the nodal method can be limited. At the same time, by choosing wisely the groups, the number of switches per groups can be limited and full-precalculation can be made. See [REF] for a detailed explanation on the SSN theory.

Within the Simulink/SimPowerSystems environment, the SSN presents some challenges for the normal user to achieve real-time simulation. The main challenge is to correctly designed the SSN model using SSN Nodal Interface Blocks to make groups of reasonable state and number of switches and to also limit the number of total nodal nodes connecting these groups.

The SSN also includes powerful features like:

1- Inlined interpolation of thyristor firing

2- Inlined Interpolation of voltage inverter in a manner similar to the RTeDRIVE models (TSB).

3- Real-time Impulse event detection.

These will be explained through a series of example.

4.2 The ssnSSN_lib.mdl library

The nss_lib library contains the nodal interface blocks along with some other utility blocks used in the SSN algorithm.

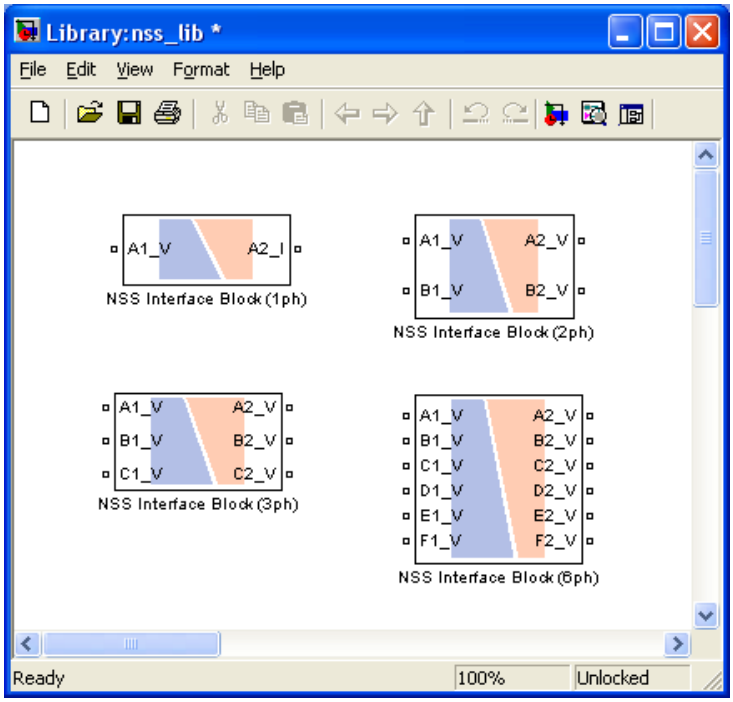


Figure 12:ssnSSN_lib library

The blocks seen in Figure 1 are called 'SSN nodal interface blocks'. They represent the nodes of the nodal method used in SSN. These SSN nodes connect state-space described groups that must respect some causality laws. For example, in state-space approach, one cannot connect a current source in series with an inductance. Similarly, the SSN nodal interface blocks must respects the same laws. To achieve this, the block port has a type I (for current source) and V (for voltage source) and this type must be chosen to respect causality laws. Taking the 1-phase SSN nodal interface block as an example: the block has an I-type port and and V-type port as selected on its dialog box below.

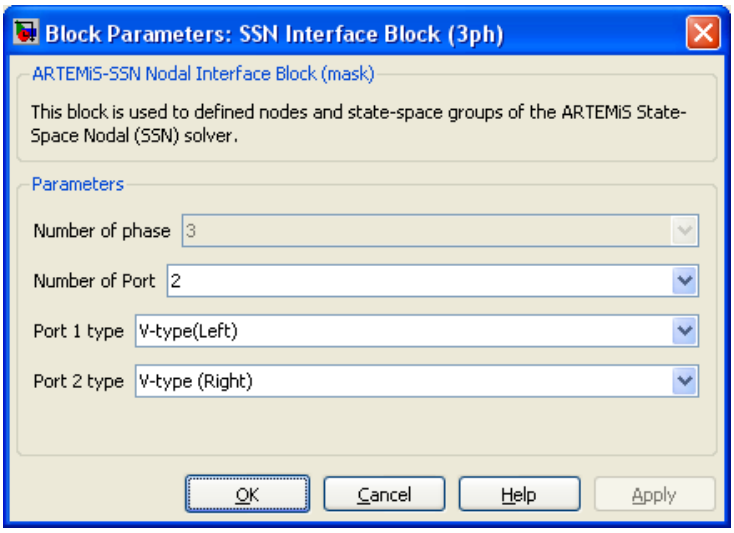


Fig 1a Dialog box of the 3-ph SSN nodal interface block

4.3 Usage of the SSN Nodal Interface Block in a model

Fig. 2 shows the usage of SSN blocks in a SPS models. The model used for this test is named 'ArtemisSSN_simple_switched_case.mdl'.

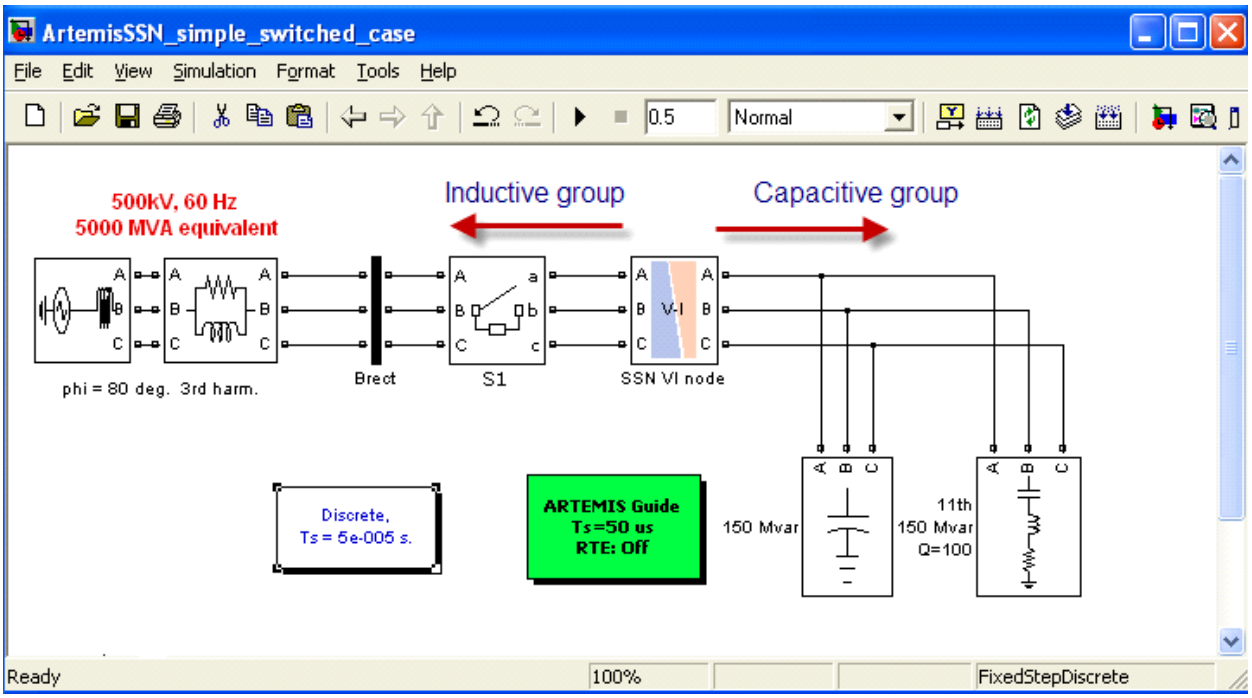


Figure 13:Example of nodal interface blocks

Some basic rules are to be followed when using the SSN blocks.

1-SSN-nodal interface block connected to inductive groups must have V-type port (view it has a Voltage source connected to an inductive element)

2-SSN-nodal interface block connected to capacitive groups must have I-type port (view it has a current source connected to an capacitive element)

3-The Main ARTEMiS Guide must have 'Enabled State-Space Nodal (SSN) method' set. Note that the solver used for the SSN method is trapezoidal like in EMTP-type software. The ARTEMiS 'Discretisation method' item only apply to part of the network that do not use the SSN solver, like the inverter side of the HVDC model of the next section.

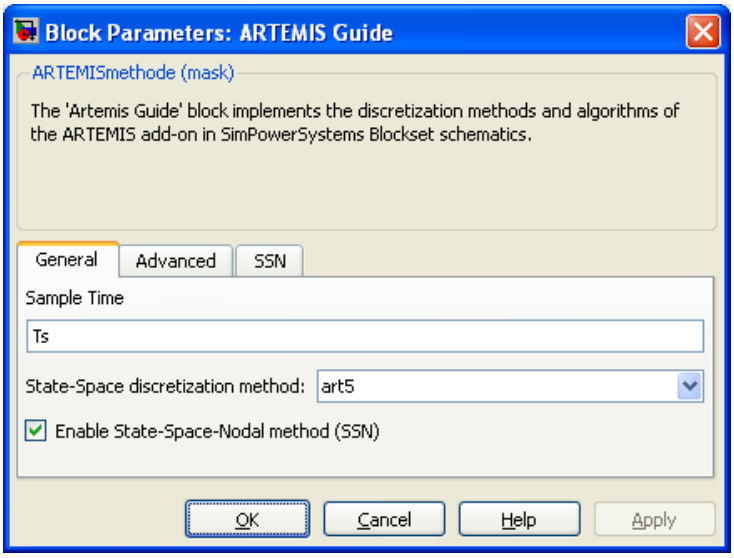


Figure 14:Fig. 3SSN and ARTEMiS block options.

4.3.1 Disabling SSN

For comparison purposes, if you disable the 'Enable State-Space Nodal method (SSN)' checkbox, the model will run using standard ARTEMiS method with the SNN nodal interface blocks still inside the model. This is because the SSN nodal interface blocks are simply null current/voltage sources that do not change the simulation when the SSN method is turned off.

4.4 1st Real-life case: 12-pulse HVDC system

The SSN method will now be shown on a 12-pulse HVDC system. The HVDC case is interesting because it offers many possibilities as how make the groups. The HVDC system is also interesting because it contains many switches: 2 6-pulse valve groups and possibly 20 or more switched filter banks on AC-bus and DC-bus. The SSN method was designed in mind to cope with this type of real-time simulation challenge.

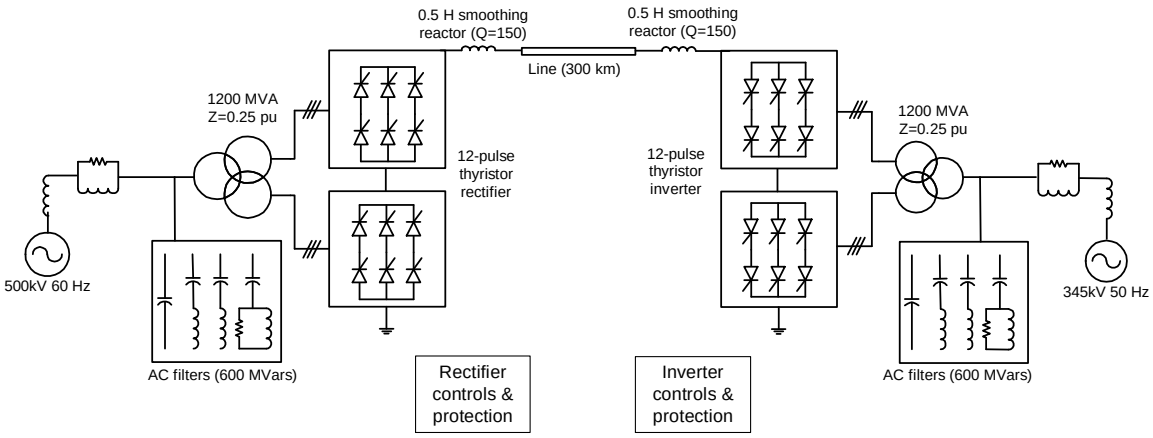


Figure 15:AD_GRID04 12-pulse HVDC model.

4.4.1 1st example of SSN groups

The most basic SSN separation we can make to use the SSN method is to use the filter bank connection point as a SSN node. Consequently, we need to understand the causality of the groups we are going to define from this (3-phase) node.

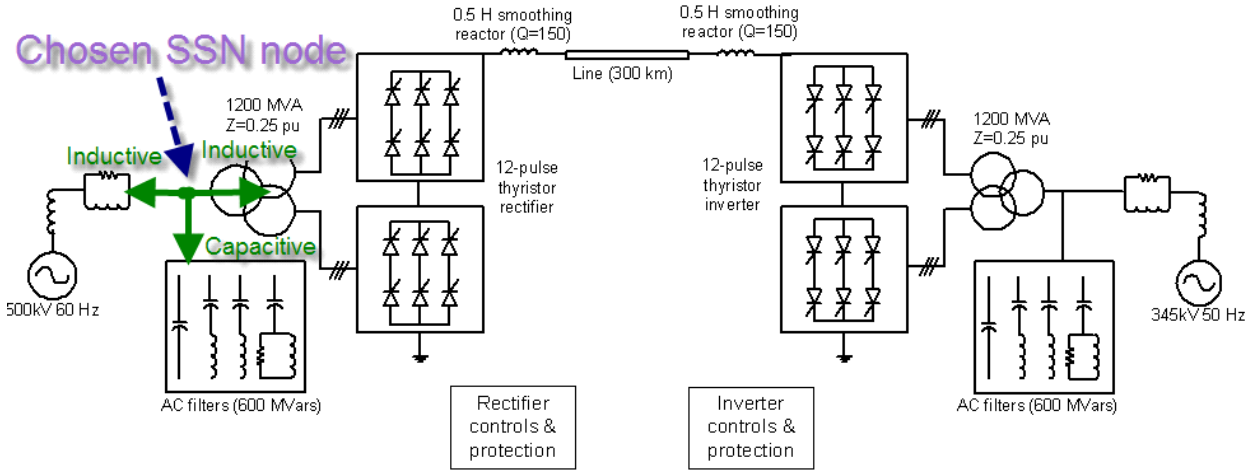


Figure 16:Interface type from the chosen SSN node

One can make the following observations: the transformer has an inductive impedance as seen from the SSN node. The source also has an inductive type impedance. Finally, the filter group has a capacitive impedance as seen from the SSN node because one of its component is a simple capacitor.

The SSN method was applied here only to the rectifier side of the HVDC system. The inverter side is still simulated by standard state-space method of SPS/ARTEMiS. The SSN could be applied also to the inverter side needless to say.

Using the filter connection point as a node, we end up with 3 SSN groups, described on the figure below.

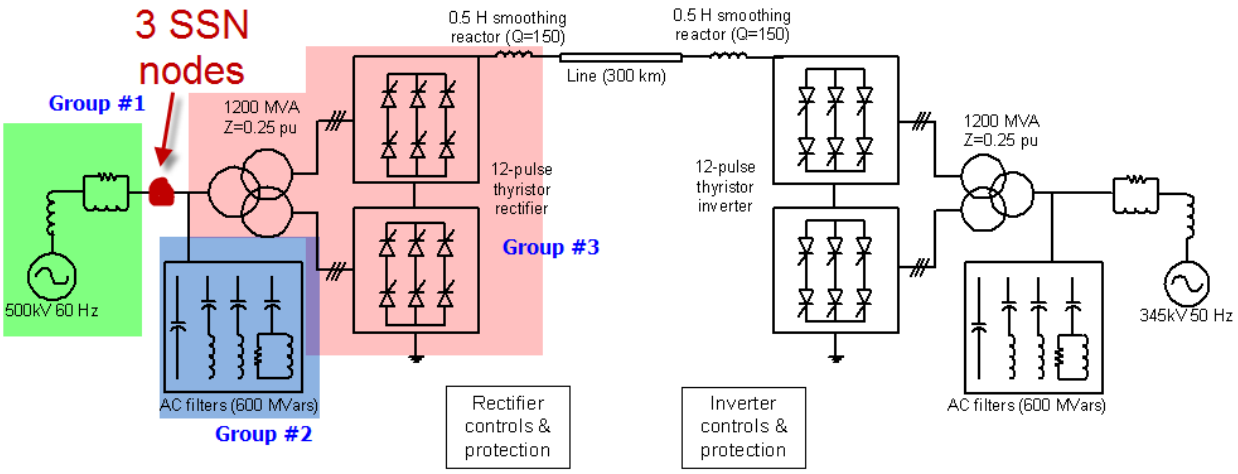


Figure 17:Resulting groups with 3 SSN nodes.

4.4.2 Adding groups

In this example, we increase the number of groups by separating the transformer from the thyristors valves, producing an additional group and 9 nodes in total. From a real-time simulation perspective, the addition of 6 nodes will slow down the simulation but separating the transformer from the valves will produce much smaller group equations. Especially, the states of the transformer will no longer have to be precomputed 2^12 times with the valves.

Also, because the thyristors have RC snubber attached to them, they are better considered as a capacitive group requiring an I-type SSN interface.

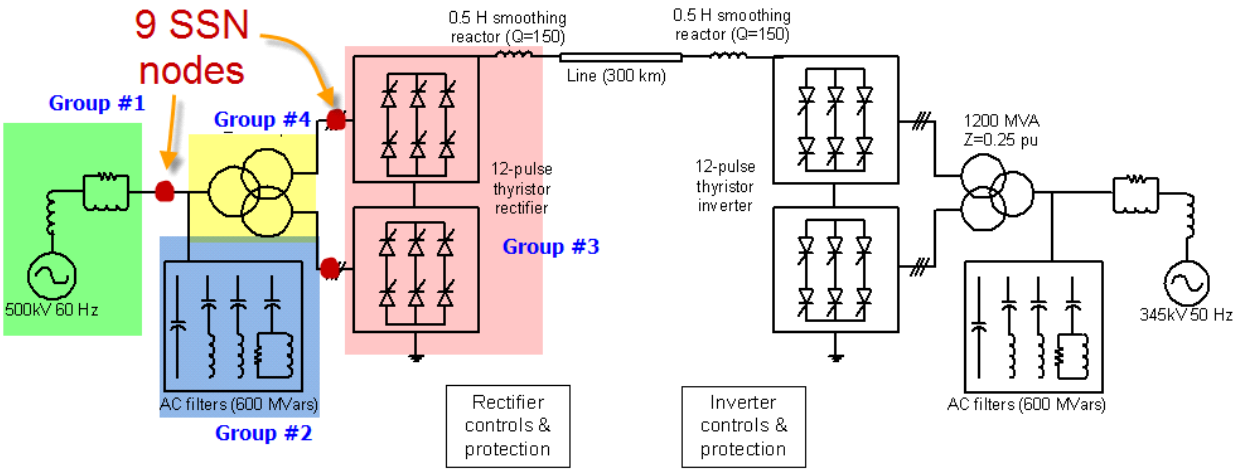


Figure 18:HVDC system with 4 groups and 9 nodes

4.4.3 Separating the valves groups

Making the two 6-pulse valves groups as 2 SSN groups has the advantage that memory requirements are minimize because there are only 2^6=64 permutations per group instead of 2^12=4096 for one 12-valve group. It may even allow the simulation to run entirely inside the L1 or L2 cache of micro-processors, so it may speed up the simulation even if we now have 11 SSN nodes.

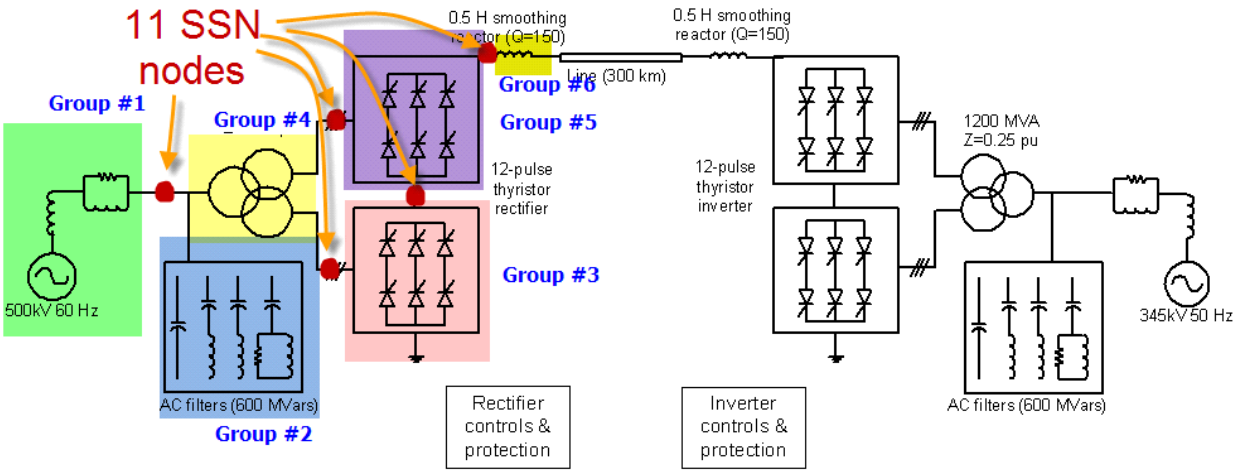


Figure 19:HVDC system with 6 groups and 11 nodes

4.4.4 Adding switched filter banks

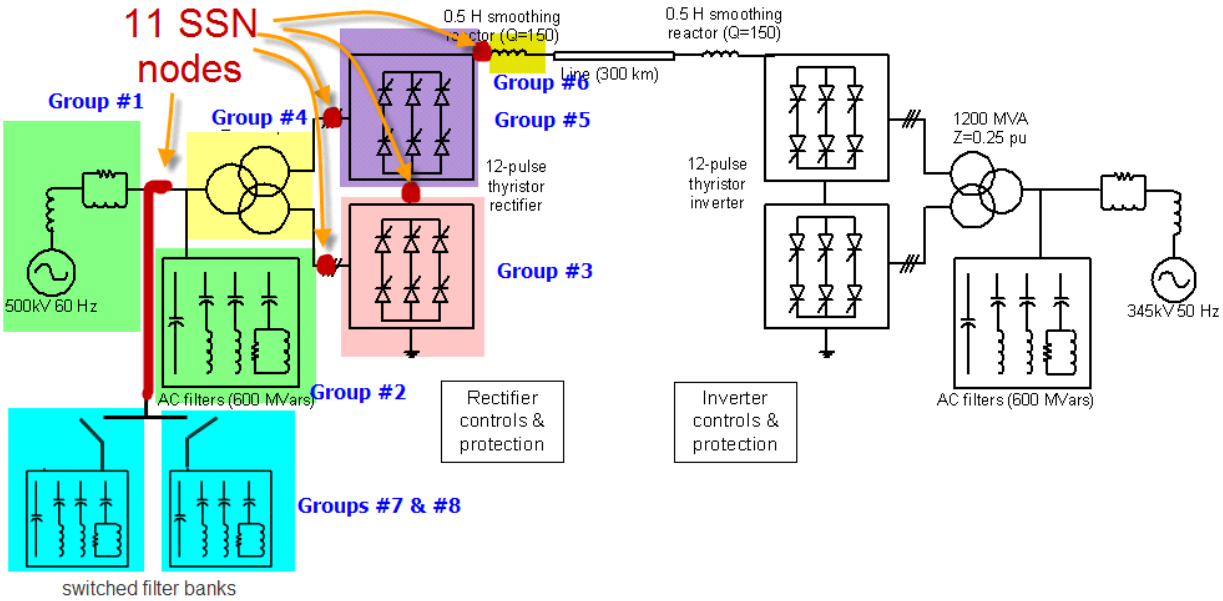


Figure 20:HVDC system with switched capacitor banks.

This last example is interesting because we added two switched filter banks to the AC-bus of the model without adding any nodes! This is caused by the facts that all the filter SSN groups (including the breakers) are connected to the nodes in the circuit.

4.5 2nd case: 3-level NCP inverter and SSN Real-Time Impulse Events

The SSN algorithm enables the detection of Impulse Events during simulation. By Impulse Event, we mean the instantaneous opening or closing of a switch (most often a diode) following the open or closing of another switch in the system. This happens for example in a buck converter in which the free-wheeling diode turn-on instantaneously when the forced switch (IGBT or MOSFET) opens.

In real-time simulation it happens that this type of event is difficult to simulate accurately. The reason is that switch natural conduction conditions are usually evaluated at the beginning of a time step, so if a forced switch change state, its effect is can only be detected on the next time step.

In ARTEMiS and ARTEMiS-SSN algorithm, we use the fact that the state of a system cannot change instantaneously when a switch changes of conduction state. We can therefore re-evaluate the switch voltage after any forced switching by simply re-evaluating the *outputs* of state equations.

In the ARTEMiS-SSN algorithm, some caution is to be taken for the Impulse Event Detection to work correctly. This is explained next.

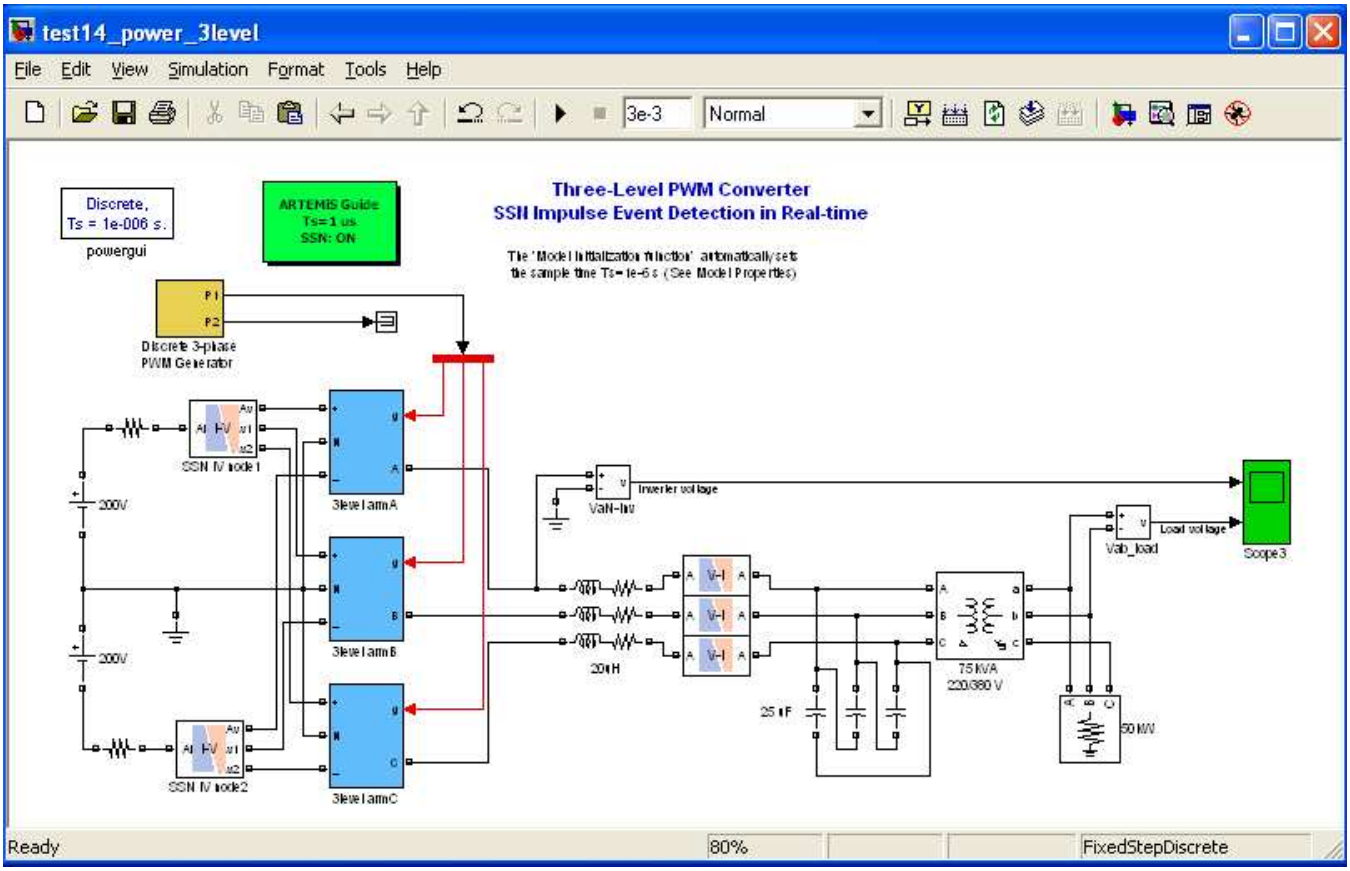


Figure 21:Three-level NCP inverter system in SSN

The above figure depicts a 3-level Neutral clamped inverter drive system in SimPowerSystems and SSN. Each arm is composed of 4 IGBT/Diode pairs plus 2 clamping diodes, each individually modeled.

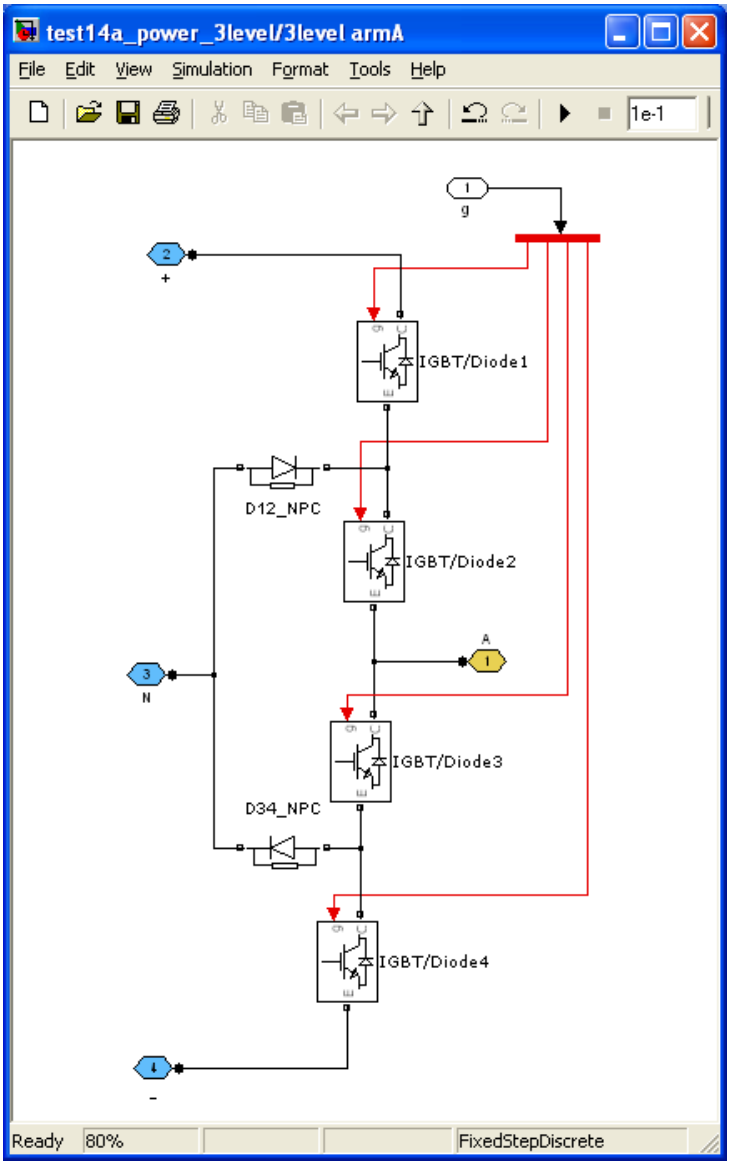


Figure 22:One arm of the 3-level NCP inverter

The real-time simulation of this model is really challenging because it is composed of 30 coupled switches. In the solution above, since SPS has a switch model for the IGBT/Diode pairs, the internal number of switches reduce to 18, which make real-time simulation still impractical because of the high number of matrix permutation to compute (2^18). The solution in SSN is to put each arm in a separate group of 10 switches (6 internal SPS switches, considering the IGBT/Diode pairs as one device).

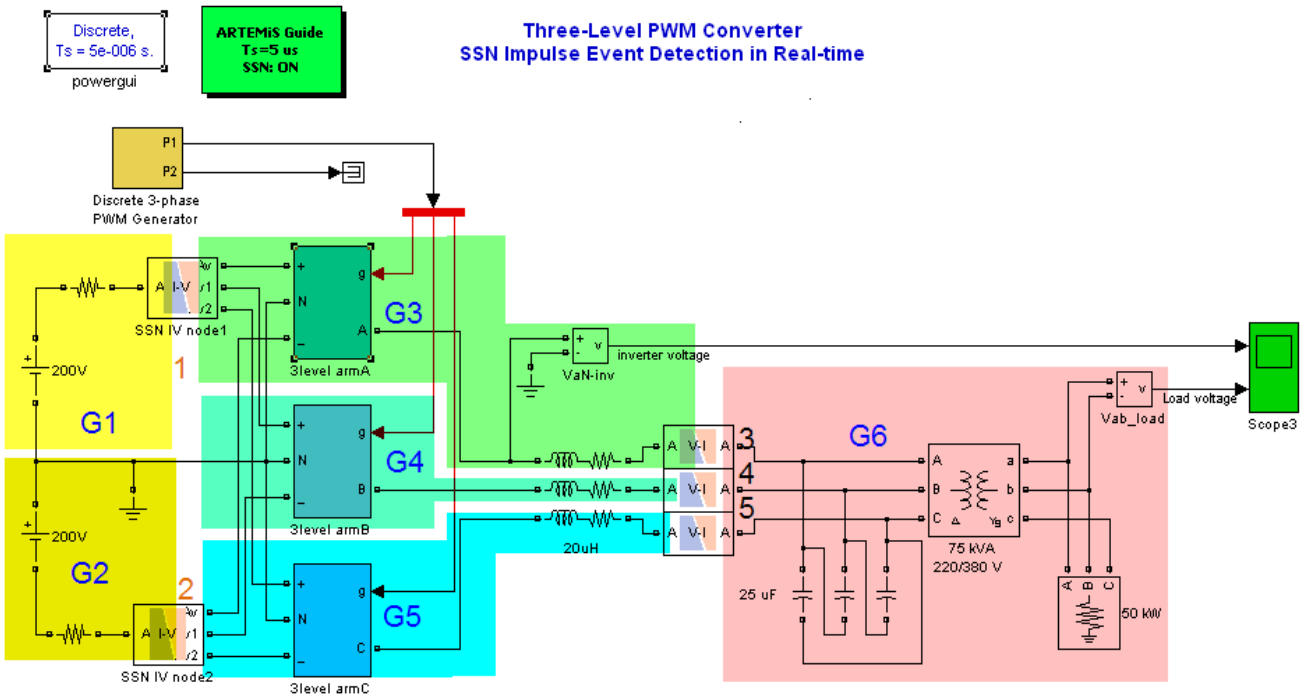


Figure 23:SSN group separation for real time simulation

The above figure shows the resulting group separation and nodal nodes. Note the following points:

1- The model has 6 groups delimited by 5 nodal connection points.

2- The inverter was separated at the arm level to obtain 6 SPS switches per group, which can be precomputed and run in real-time after.

3- The 'Ground' acts as a natural separation point and does not require a SSN Nodal Interface Block. That is why groups G1 and G2 are separated.

4- The load inductive branch was included WITH the inverter arm. This is necessary for the Impulse Event Detection to work correctly in SSN.

4.5.1 Impulse Events in SSN

This last point is important to understand. It is caused by the fact that the SSN algorithm does not make multiple iteration of equation to verify Impulse Events like instantaneous diode turn-on effects. It only re-evaluate the Outputs of a group for natural switch threshold crossing each time a forced switch is activated. This can be done on the basis that the states of a systems cannot change instantaneously on a switching action.

In general, a switched device using diodes as free-wheeling diode (for example) will have a branch that force the continuity of the current at switching time. This element must be grouped with the switching elements for the SSN Impulse Event Detection to work. In the example of the 3-level NCP inverter, this element is the inverter output inductor.

Consider for example the case in which Phase A current is positive and IGBT/Diode1 and IGBT/Diode2 are conducting. When IGBT1 is turned OFF, NPC Diode D12_NPC turns ON instantaneously because of the load inductance.

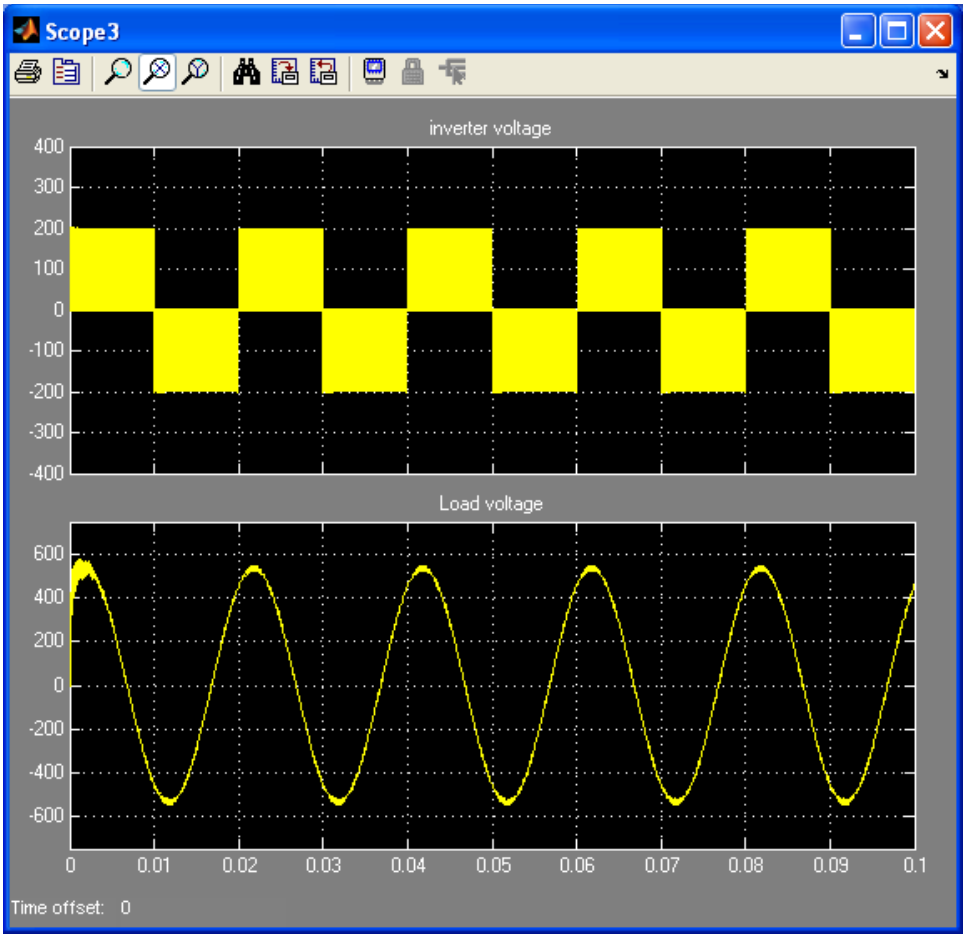


Figure 24:Simulation results of the 3-level NCP inverter system using SSN at 5 µs

4.6 3rd case: Inlined Thyristor Valve Compensation in SSN

The Inlined Thyristor Valve Compensation (ITVC) method is a real-time method to compensate the sampling effect of thyristor by the fixed step time frame. Simply explained, each time a thyristor firing pulse is generated, it must 'wait' the next time step to be taken into account inside the simulation. If the pulse arrive just before the fixed step frame, the error is minimal but when it occurs just after, then the error is bigger because the wait last almost a full time step. Because the firing pulse are not synchronized on the simulation time step, it usually results in a low-frequency jitter on important system variable, often confused with controller instability.

The ITVC methods is designed to compensate this effect, in off-line and HIL simulation. It is so efficient that it is always active in the ARTEMiS (State-Space and SSN).

We will explain the ITVC method on the HVDC example with 6 groups, 11 nodes SSN separation.

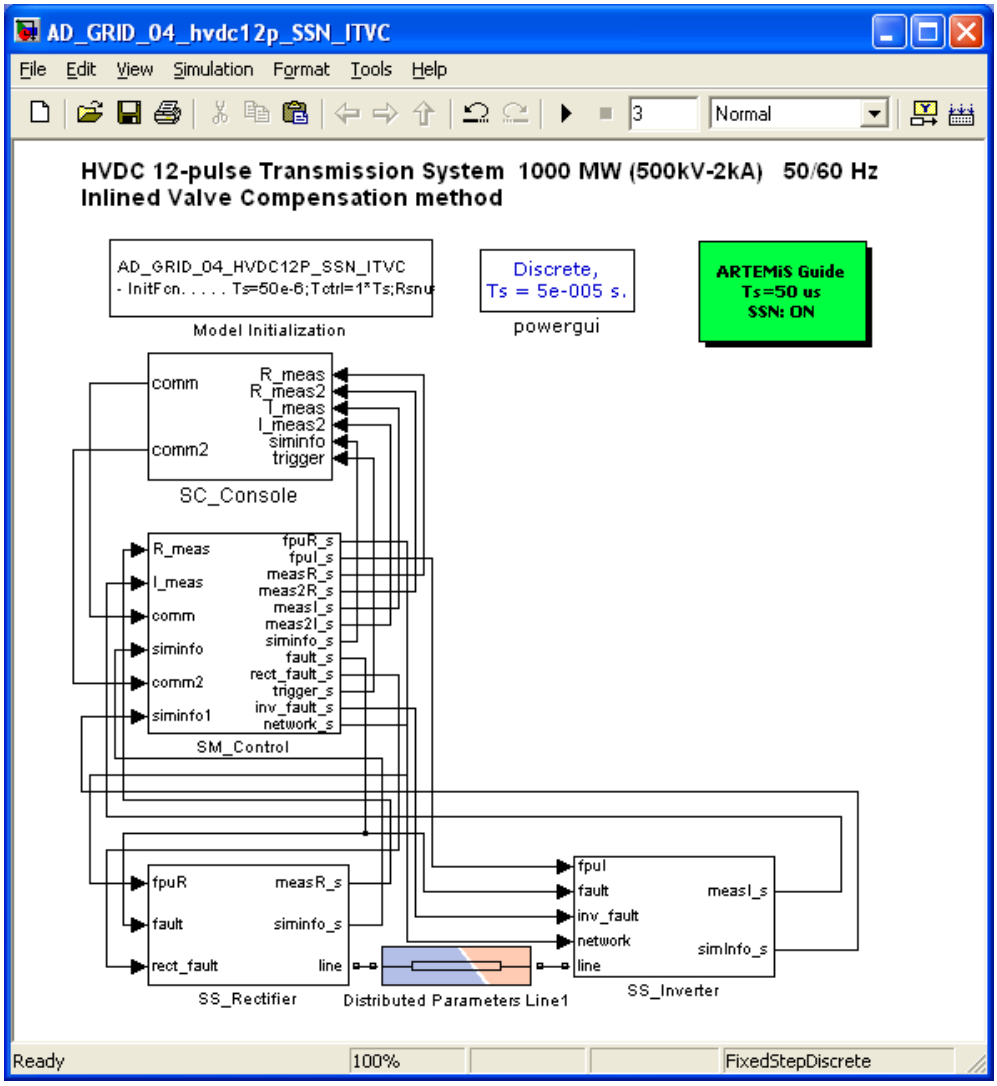


Figure 25:HVDC system with ITVC (RT-LAB top level separation in 3 CPUs)

In the model, a Firing Pulse Unit was designed with RT-Events, a replica of the Simulink FPU with RTE blocks.

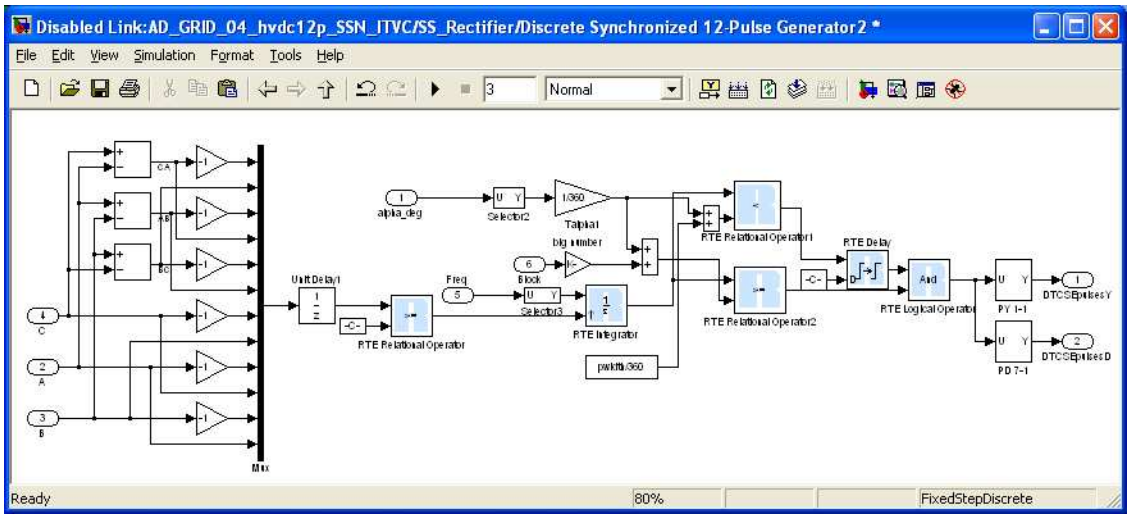


Figure 26:RT-Events based Firing Pulse Unit

The RT-Events blockset enables to keep in memory the in-step events of this type of firing pulse unit with multiple comparators.

Since release 6 of ARTEMiS, the way RT-Events connects to ARTEMiS solvers has been simplified. The ARTEMiS solver now requires only a double value between zero and 1 to activate and compensate thyristors switches. If the value equal only exactly 1 and 0 (as in regular SPS), the simulation is not compensated. But if the value is between 0 and 1, the value is taken as the time ratio of the gate event within the time step. Ex: a value of 0.6 would mean that the event occurred at 60% after the beginning of the time step.

Now, in common model a simple 'RTE converter' block will do this jog as in the following figure. If and only if the RT-Events compensation item of the block is set to 'Enabled', the HVDC simulation will also be compensated.

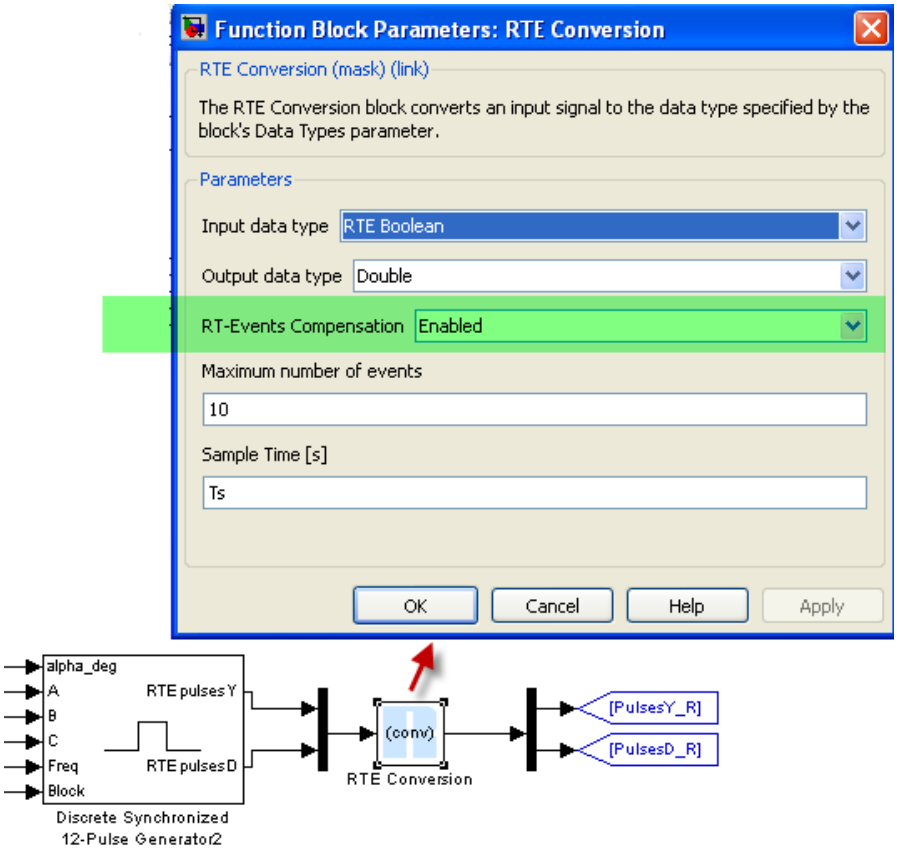


Figure 27:Interface of RT-Events and ARTEMiS (V6 and later)

The ITVC algorithm action is very impressive considering it overall negligible computational cost. The following figure shows the DC current of the HVDC during energization.

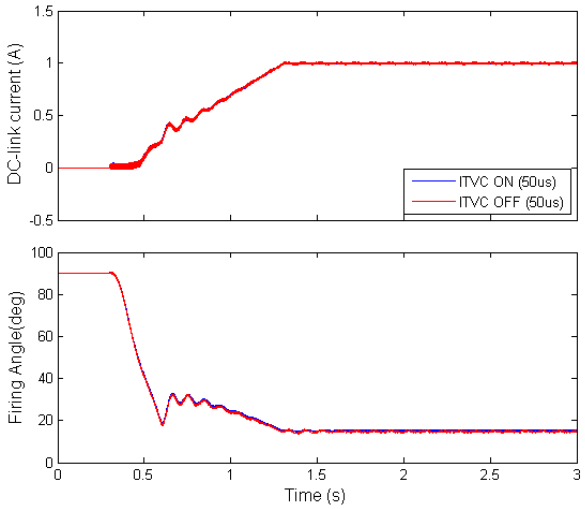


Figure 28:HVDC energization

If we now look closer at the Idc current and rectifier firing angle, the effect of the compensation is quite obvious.

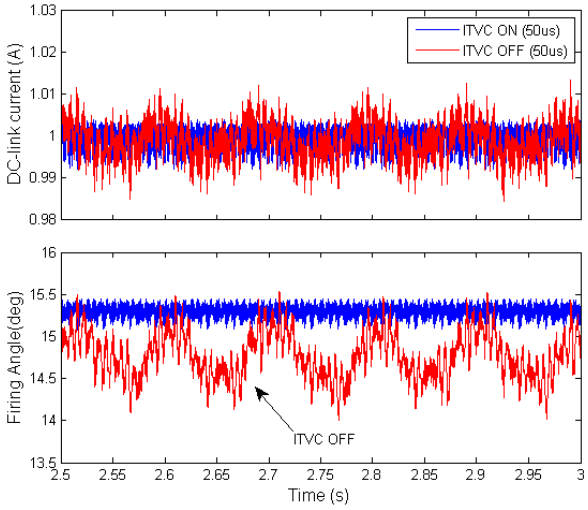


Figure 29:Zoom on DC-link current and firing angles at of the rectifier side

On the above figure, we observe a very characteristic low-frequency jitter on both DC-link current and firing angle, quantities linked by the HVDC control. When the ITVC is OFF, there is a approx. 10 Hz jitter on both values that is not present with ITVC in function. This jitter is typical of fixed-step solvers and would be present in all fixed-step based simulation algorithms (EMTP, PLECS, SPS, PSIM, etc...).

4.7 Static Var Compensator

A 300-Mvar Static Var Compensator (SVC) regulates voltage on a 6000-MVA 735-kV system. The SVC consists of a 735kV/16-kV 333-MVA coupling transformer, one 109-Mvar thyristor-controlled reactor bank (TCR) and three 94-Mvar thyristor-switched capacitor banks (TSC1 TSC2 TSC3) connected on the secondary side of the transformer. Switching the TSCs in and out allows a discrete variation of the secondary reactive power from zero to 282 Mvar capacitive (at 16 kV) by steps of 94 Mvar, whereas phase control of the TCR allows a continuous variation from zero to 109 Mvar inductive. Taking into account the leakage reactance of the transformer (15%), the SVC equivalent susceptance seen from the primary side can be varied continuously from from -1.04 pu/100 MVA (fully inductive) to +3.23 pu/100 Mvar (fully capacitive). The SVC controller monitors the primary voltage and sends appropriate pulses to the 24 thyristors (6 thyristors per three-phase bank) in order to obtain the susceptance required by the voltage regulator [1].

Each three-phase bank is connected in delta so that, during normal balanced operation, the zero-sequence tripplen harmonics (3rd, 9th...) remain trapped inside the delta, thus reducing harmonic injection into the power system. The power system is represented by an inductive equivalent (6000 MVA short circuit level) and a 200-MW load. The internal voltage of the equivalent can be varied by means of programmable source in order to observe the SVC dynamic response to system voltage sags.

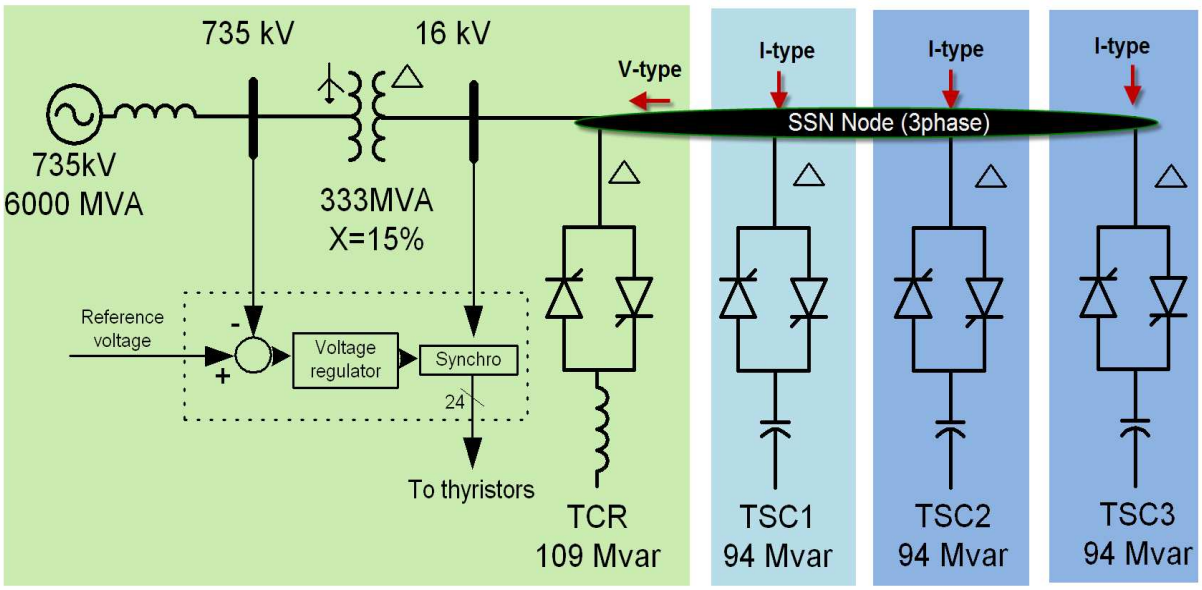


Figure 30:SVC compensated electric network

With the SSN solver, the natural way to decouple the system is to use the common connection point of the TCR and the 3 TSCs, resulting in 4 groups of 6 switches each and nodal matrix of size 3 only, thus very efficient in computational terms. The TCS groups are interfaced with I-type SSN Nodal Interface Blocks while the TCR and network group is interfaced with a V-type block (hint: it is clearly inductive so it must be driven by a Voltage source for causality reasons ->V-type).

With the ITVC compensation of thyristor firing, very accurate simulation ca be achieved. The above figure shows the simulation results for a slow scan of the TCR bank firing angle. The figure below shows a typical effect of thyristor-based system in fixed step simulation. In that case, a kind of quantization effect occurs on the system

output reactive power, as it shows some discrete step effects. With the ITVC compensation of ARTEMiS and SSN, the reactive output of the systems is smooth with regards to the firing angle.

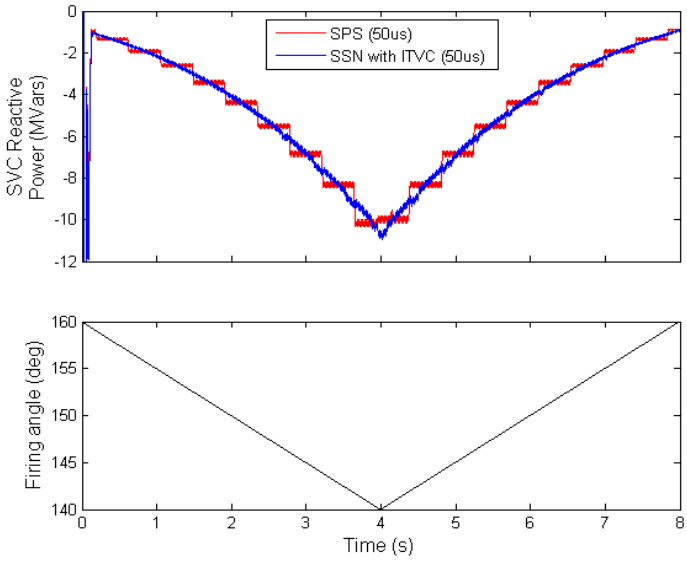


Figure 31:Effect of firing compensation in ARTEMiS

Obtaining FD-line model parameters from EMTP-RV

Here you can find procedure to obtain FD-Line model parameters from EMTP-RV :

Obtaining_FDline_model_parameters_from_EMTP_RV.pdf

Reference

5

This section describes the various blocks and functions provided with ARTEMiS.

Library

ARTEMiS (Advanced Real-Time ElectroMagnetic Simulator)

Block

The ARTEMiS Guide block is the main discrete simulation parameter control block of ARTEMiS from which the different ARTEMiS solvers can be selected.

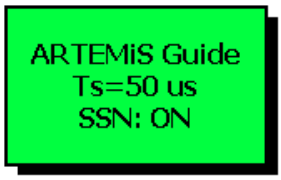


Figure 32:ARTEMiS Guide Block

Mask

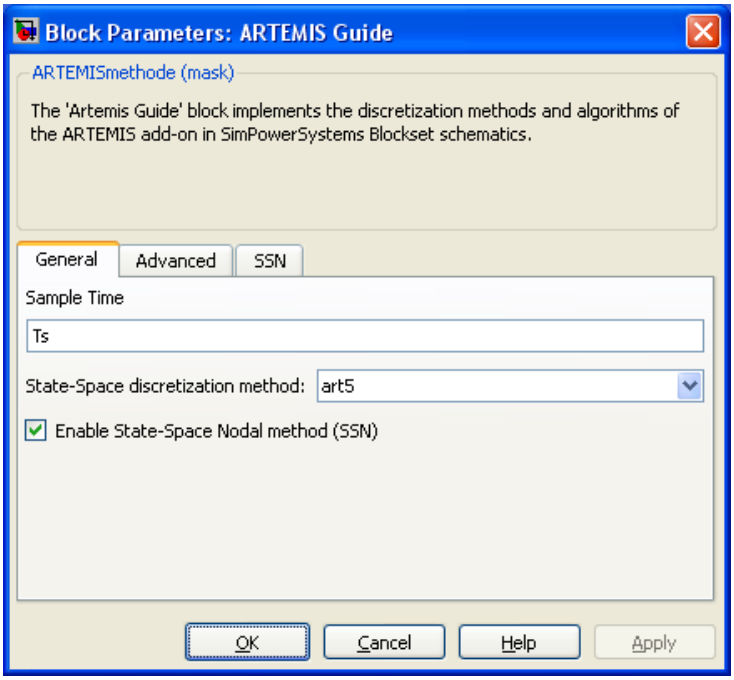


Figure 33:Mask of the ARTEMIS Guide Block

Description

The ARTEMiS Guide block is used to discretize the linear part of the state-space system generated by the SimPowerSystem blockset (SPS). It implements strictly fixed time step simulation of SPS schematics and offers alternative to the Tustin discretization method of the SPS to increase numerical stability and precision. In contrast to the simulation technique

of the SPS, the 'ARTEMiS Guide' block precomputes and discretizes all state-space matrices for all combinations of the switch topologies thus permitting hard real-time simulation.

Since v6, ARTEMiS offers a new simulation algorithm called State-Space Nodal (SSN), which combines the advantages of state-space methods with regards to the accuracy of discretisation and switch management of nodal methods.

Since v6 also, the interpolation method have been changed to ’Inlined’ methods which are more efficient in terms of calculation and more easy to use. The term ’Inlined’ refers to the facts that the method is implemented using only one line in the code! The interpolation methods are now active by default because of their simplicity.

Parameters

General tab

Sample Time (s): Sets the sample time for the fixed time step simulation of the electrical part of the SPS model.This sample time should be the same as the one entered in the SPS PowerGUI block.

State-Space discretization method: Sets the discretization method used by the ARTEMIS algorithm *for the normal state-space system, not the one using SSN method*. Four different methods are available:**art5 (default)**, **art3**, **art3hd** and **trapezoidal**. The **art5** and **art3** discretization methods are highly stable and very-accurate integration methods. Both are immune to numerical oscillations caused by switch operations in power networks. The **art5** method is theoretically more accurate than **art3**, as it approximates the matrix exponential Taylor expansion to the 5th term, while **art3** and **trapezoidal** approximate to the 3rd and 2nd terms, respectively. The **art3hd** discretization methods a highly-stable method with good precision, especially in highly non-linear networks like the demo example provides with SPS called power_surgnetwork. mdl. The **art3hd** method is the only integration method capable of simulating the power_surgnetwork.mdl model with a time step greater than 90us.

Enable State-Space Nodal method: When checked, activates the use of SSN methods in SPS subsystems where nodal nodes have been defined using SSN *Nodal Interface Blocks*.

Advanced tab

Dynamic calculation of switch pattern matrix permutations: (DCSPMP) This parameter allows ARTEMiS to dynamically compute the state-space matrices caused by the switch permutations of the electrical system *during* the real-time simulation. The state-space matrices are stored in memory cache as they occur. This way, the next time the same topology of switch occurs, the corresponding state-space matrices are retrieved from the cache without overhead.

In simulation cases where the switch pattern is cyclical, like in steady-state operation of converter-rectifier circuits, hard real-time simulation can be achieve easily if the *Maximum number of cached switch pattern matrix permutations* parameter is set greater than the number of topology of switch patterns that *actually* occur during the simulation.

This option is useful in simulation cases where the number of switch would cause precomputation to require unreasonable amount of RAM memory if all permutations are precomputed.

NOTE: this parameter only affects the regular state-space simulation (i.e. not SSN). Furthermore the use of DCSPMP disables the detection of Impulse Events (instantaneous diode turn-on effects) in the simulation. Does not apply to SSN.

Maximum number of cached switch pattern matrix permutations: This parameter determines the maximum number of topology of the system to be stored in memory when the dynamic calculation is enabled.

To set ideas, a circuit with 3 switches requires 2^3=8 cached switch pattern matrix permutations to hold the complete sets of state-space matrix for that system.

Use full precomputation of state-space matrix for real-time simulation only: this option allows full matrix precalculation on the target only. This option is usefull to rapidly obtain offline simulation results on a host PC with a limited amount of RAM memory and at the same time allow full matrix precomputation on the targets to effectively obtain real-time computation performances.

Use continuous time machine models: this option will force SPS to use continuous-time machine models inside the fixed-step simulation scheme. The machine are modeled with Laplace integrators and the main Simulink fixed-step solver (ode1 to ode5) will be used to iterate the machine models.

Show Load flow Options: this option is used to conveniently substitute SPS model to calculate load flow by the SPS Load Flow routine. Neither the ARTEMiS Line model is nor the standard SPS RLC load blocks are recognized by the SPS load flow routine. This items enables the Distributed Parameter Line model type and RLC load substitution by Dynamic Load model that allows correct model substitution.

Distributed Parameter Line model type: this option allow to swap between ARTEMiS DPL model or SPS DPL model. Only the latter one can be used for load flow calculations. The ARTEMiS Distributed Parameter Line models are required to enable the parallel simulation of subnetworks separated by them in the RT-LAB framework.

RLC load substitution by Dynamic Load model: SPS RLC load blocks can be automatically substitute by a Dynamic Load model with the same power settings to facilitate load flow calculations.

SSN tab

SSN solver: type of solver used for the SSN method. The SSN algorithm solve a model as two parts: state-space groups connected in a nodal method. The state-space groups can be solved by state-space discretisation similar to standard ARTEMiS, while the nodal part can be solved by Trapezoidal, Backward Euler or Balanced-zero-hold, a mix of Backward and Forward Euler. The default method is *Trapezoidal.* Other methods are provided for help only. In case of numerical oscillations at nodal connection points, the Art5 or Backward Euler method can provide a solution.

Note that if the ARTEMiS-SSN Frequency Dependent Parameter line is used in the model, the Trapezoidal solver must used (because it is used internally by this model)

Inputs

None

Outputs

None

Characteristics and Limitations

Number of switches in ARTEMiS state-space solvers

The SSN method main purpose is to uplift the limitation on the number of switches that a model can contain in state-space approach. There is always a SSN group separation method that will allow full pre-calculation of all matrices and real-time simulation. Switches can even be in a group by themselves. The following explanation therefore only apply to system *NOT* modeled with the SSN approach.

In regular (non-SSN with full matrix pre-computation), ARTEMiS allocate memory and pre-compute ABCD matrix sets for all permutations of switch positions. For a system with nb_sw switches, this produces 2^nb_sw ABCD matrix sets. The maximum number of switch that can be present is 24. Depending on the electric system size and the number of switches in the network, the computer may not have enough space to allocate all the required memory and a Simulink 'Memory allocation error' will occurs. In this mode, the solution is either to remove some switches or to enable **Dynamic calculation of switch pattern matrix permutations** option.

The **Dynamic calculation of switch pattern matrix permutations** option pre-allocates a block of RAM memory to store ABCD matrix sets for a priori unknown switch permutations in ARTEMiS (determined during simulation and computed on-the-fly) and is also limited by the computer main memory size. Although the theoretical maximum number of **Maximum number of cached switch pattern matrix permutations** is equal to 2^24, no real PC have enough memory to allocate such a large quantity of ABCD matrix set. If this option produces a Simulink 'Memory Allocation Error', it means that the number is too large for the RAM memory of the PC in use and the number should be diminished. The maximum number of **Maximum number of cached switch pattern matrix permutations** depends on the size of the network simulated. It will be smaller for large networks. Typical values range from 2^12 to 2^15 on 2GB PC.

Number of switches in ARTEMiS-SSN solvers

With the ARTEMiS-SSN solver, the switch limitation is waived but the user must create groups with a limited number of switches to limit memory usage by the stored matrix permutation of the groups. The **SSN-solver does *not* have Dynamic Calculation of switch pattern matrix permutation** so switch number should be limited to reasonable number (12 and lower for example per SSN group)

Interpolation methods

ARTEMiS v6 and later automatically incorporates many interpolation methods that were previously manually enabled. There are 3 types of interpolation implemented in ARTEMiS:

Impulse Event Detection: This type of interpolation occurs when a forced switch action instantaneously induce a limit condition on another natural switch like a diode. A good

example of this is in buck converter where the opening of a IGBT instantaneously put the free wheeling diode in conduction. This type of event is now supported by default in ARTEMiS v6 and later.

Inlined Thyristor Valves Compensation (ITVC, ITVC-SSN): this algorithm corrects the firing jitter of thyristor valves caused by fixed step sampling of the gate signals. It automatically activates if the gate signal is a double number ranging continuously from 0 to 1. The number (ex: 0.458) indicates the in-step delay since the last sample time. The method deactivates if the number is the usual binary number used to control switches. The method is implemented in both state-space and SSN algorithms.

Inlined Voltage Inverter Compensation (IVIC-SSN): available in SSN only, the IVIC-SSN method will compensate the simulation of voltage inverter modeled with SPS Universal Bridge blocks in a matter equivalent to RTeDrive TSB blocks. It automatically activates if the gate signal is a double number ranging continuously from 0 to 1. The number indicates the in-step delay since the last sample time. The method naturally account for all working modes of the inverter, including high impedance case. It must be used in conjunction with a SSN-defined load (motor, filter, etc....) to work correctly.

Direct Feedthrough	N/A
Discrete sample time	Yes
RT-LAB XHP support	Yes
Work offline	Yes

Related Items

ARTEMIS Distributed Parameters Line, ARTEMiS Stubline, ARTEMiS-SSN Nodal interface Blocks.

Library

ARTEMIS

Block

The ARTEMIS distributed parameters line block implements an N-phases distributed parameters transmission line model optimized for real-time simulation.

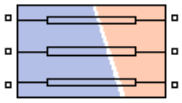


Figure 34:ARTEMIS distributed parameters line block

Mask

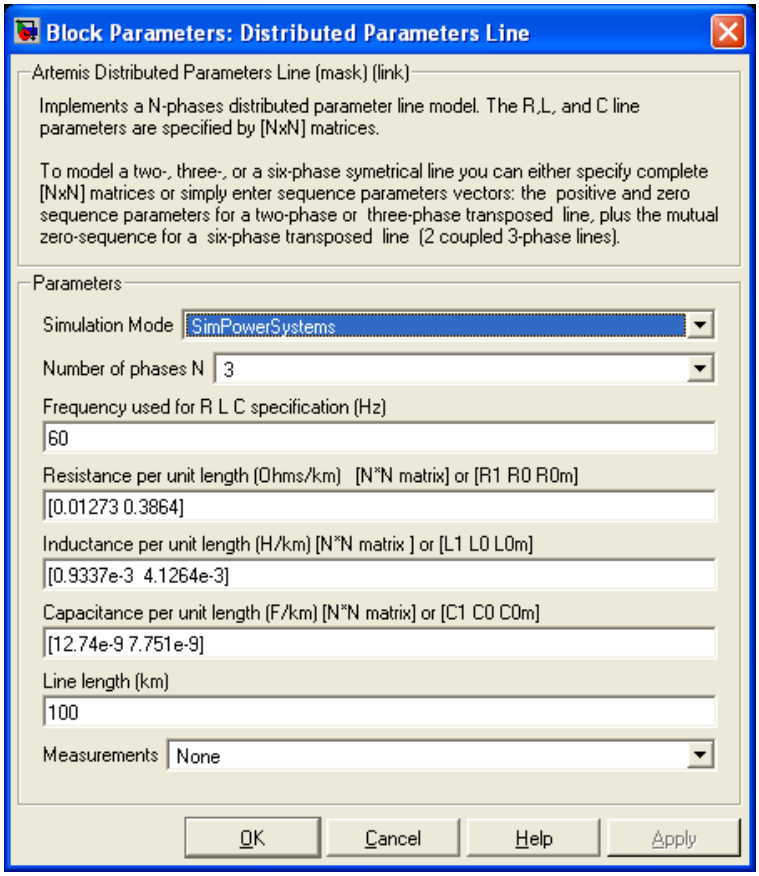

Block Parameters: Distributed Parameters Line
Artemis Distributed Parameters Line (mask) (link)
Implements a N-phases distributed parameter line model. The R,L, and C line parameters are specified by [NxN] matrices.
To model a two-, three-, or a six-phase symetrical line you can either specify complete [NxN] matrices or simply enter sequence parameters vectors: the positive and zero sequence parameters for a two-phase or three-phase transposed line, plus the mutual zero-sequence for a six-phase transposed line (2 coupled 3-phase lines).
Parameters
Simulation Mode
SimPowerSystems
Number of phases N
3
Frequency used for R L C specification (Hz)
60
Resistance per unit length (Ohms/km) [N*N matrix] or [R1 R0 R0m]
[0.01273 0.3864]
Inductance per unit length (H/km) [N*N matrix] or [L1 L0 L0m]
[0.9337e-3 4.1264e-3]
Capacitance per unit length (F/km) [N*N matrix] or [C1 C0 C0m]
[12.74e-9 7.751e-9]
Line length (km)
100
Measurements
None
OK
Cancel
Help
Apply

Figure 35:Mask of the ARTEMIS distributed parameters line block

Description

The ARTEMIS Distributed Parameters Line block implements an N-phases distributed parameters line model with lumped losses. The model is based on the Bergeron's travelling wave method used by the Electromagnetic Transient Program (EMTP) **[1]**. This block is similar to the SPS distributed parameters line block but is optimized for discrete real-time

simulation and allows network decoupling. It also allows multi-CPU simulation on an RT-LAB simulator.

Refer to the SPS Distributed Parameter Line block Reference page for more details on the mathematical model of the distributed parameters line.

ARTEMIS provides an m-script that converts the SPS distributed parameters line block to an ARTEMIS distributed parameters line block. See the **ARTEMIS Distributed Parameters Line** reference page for more details on this script.

Network decoupling

One of the main advantage of the ARTEMIS line blocks (Distributed parameters lines and Stublines), by opposition to the SPS lines, is the decoupling of the electric circuit into smaller subnetworks. This important property allows ARTEMIS to simulate, in real-time, circuit with more switching elements.

SPS and ARTEMIS solve electric circuits using the common state-space method. One of the main limitation of this method is related to the switch elements. When an event occurs that changes the topology of the circuit (or change the state of a switch), SPS and ARTEMIS need to compute a new state-space matrix. This calculation causes a non acceptable overhead when simulating a circuit in real-time.

To solve this problem, ARTEMIS stores the state-space matrices of a given set of topologies, normally the steady-state topologies, in cached memory and uses them when necessary without having to recalcule the matrices. However, the number of matrices required to cover all topologies of the system depends on the number of switch elements. When a circuit contains a lot of switch elements, the number of required topologies is high and it is not possible to store all matrices in cached memory because of the size of the matrices.

The decoupling property of the line allows ARTEMIS to divide the state-space system in two different state-space systems and reduce the total size of the state-space matrices in memory. It also reduces the maximum number of topologies by an important factor.

RT-LAB simulation using a cluster of PCs

The distributed configuration of RT-LAB allows for complex models to be distributed over a cluster of PCs running in parallel. The target nodes in the cluster communicate between each other with low latency protocols such as shared memory, FireWire, SignalWire or InfiniBand, fast enough to provide reliable communication for real-time applications.

However, electrical circuit cannot be easily distributed over a cluster of PCs without changing the dynamic behaviors of the system. The communication delays degrade the computation.

ARTEMIS lines (Distributed Parameters Lines and Stublines) can be used to distribute a circuit over a cluster of PCs. ARTEMIS used the intrinsic delay of the line to split the circuit without affecting the dynamic property of the system. Moreover, SPS and ARTEMIS use physical modelling lines and connectors to model the circuit. This type of signals cannot be used by RT-LAB to communicate signals between subsystems, because the RT-LAB opcomm block only supports basic Simulink signals. The only exception to this rule are the ARTEMIS **Distributed Parameters Line** block and the ARTEMIS **Stubline** block. RT-LAB allows the insertion of a line block at the root level of the block diagram and the connection of the physical modelling ports of the block to the real-time subsystems. Also note that the physical modelling signals and ports do not have to pass through the opcomm block. The Example in the *Characteristics and Limitations* section illustrates how to use the block with RT-LAB.

Parameters

Simulation mode: Defines the mathematical models of the distributed parameters line used by ARTEMIS and SPS. Here are the available options:

- SimPowerSystems: When this option is selected the block uses the SPS mathematical model that is not optimized for real-time simulation.
- ARTEMIS model: When this option is selected the block uses the ARTEMIS mathematical model that allows fast real-time simulation and that allows network decoupling.

Number of phases N: Specifies the number of phases, N, of the model. The block dynamically changes according to the number of phases that you specify. When you apply the parameters or close the dialog box, the number of inputs and outputs is updated.

Frequency used for RLC specifications: Specifies the frequency used to compute the resistance R, inductance L, and capacitance C matrices of the line model.

Resistance per unit length: The resistance R per unit length, as an N-by-N matrix in ohms/km. For a symmetrical line, you can either specify the N-by-N matrix or the sequence parameters. For a two-phase or three-phase continuously transposed line, you can enter the positive and zero-sequence resistances [R1 R0]. For a symmetrical six-phase line you can set the sequence parameters plus the zero-sequence mutual resistance [R1 R0 R0m]. For asymmetrical lines, you must specify the complete N-by-N resistance matrix.

Inductance per unit length: The inductance L per unit length, as an N-by-N matrix in henries/km (H/km). For a symmetrical line, you can either specify the N-by-N matrix or the sequence parameters. For a two-phase or three-phase continuously transposed line, you can enter the positive and zero-sequence inductances [L1 L0]. For a symmetrical six-phase line, you can enter the sequence parameters plus the zero-sequence mutual inductance [L1 L0 L0m]. For asymmetrical lines, you must specify the complete N-by-N inductance matrix.

Capacitance per unit length: The capacitance C per unit length, as an N-by-N matrix in farads/km (F/km). For a symmetrical line, you can either specify the N-by-N matrix or the sequence parameters. For a two-phase or three-phase continuously transposed line, you can enter the positive and zero-sequence capacitances [C1 C0]. For a symmetrical six-phase line you can enter the sequence parameters plus the zero-sequence mutual capacitance [C1 C0 C0m]. For asymmetrical lines, you must specify the complete N-by-N capacitance matrix.

Line length: The line length, in km.

Measurements: Line current and voltage measurement are not working.

Inputs

N-Phases voltage-current signals

Outputs

N-Phases delayed voltage-current signals.

Characteristics and Limitations

The ARTEMIS distributed parameters line block does not initialize in steady-state so unexpected transients at the beginning of the simulation may occur.

The use of the ARTEMIS Distributed Parameter Line disable the 'Measurements' option of the regular Distributed Parameter Line. Usage of regular voltage measurement blocks is a good alternative.

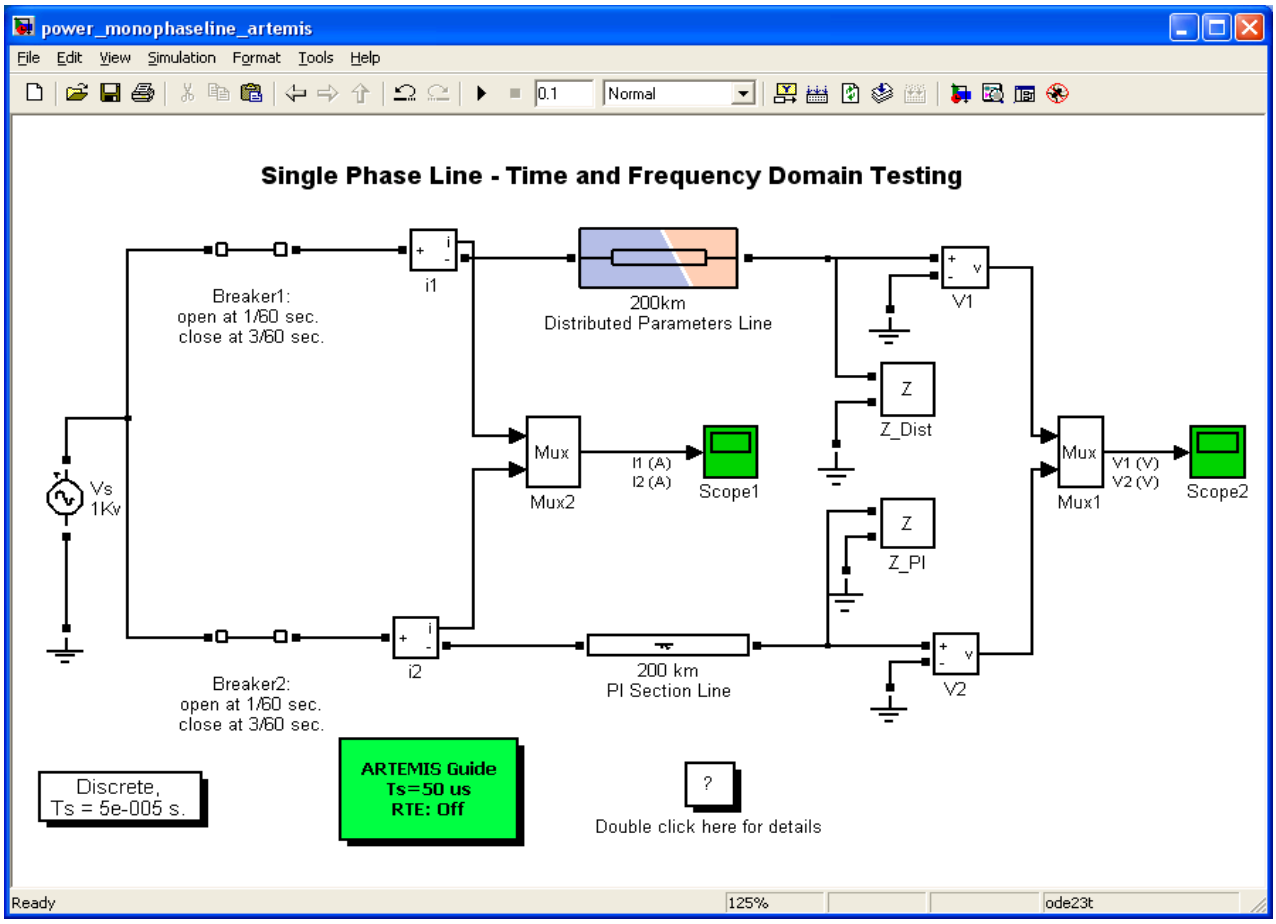
Direct Feedthrough	No
Discrete sample time	Yes, defined in the ARTEMIS guide block.
XHP support	Yes
Work offline	Yes

Example

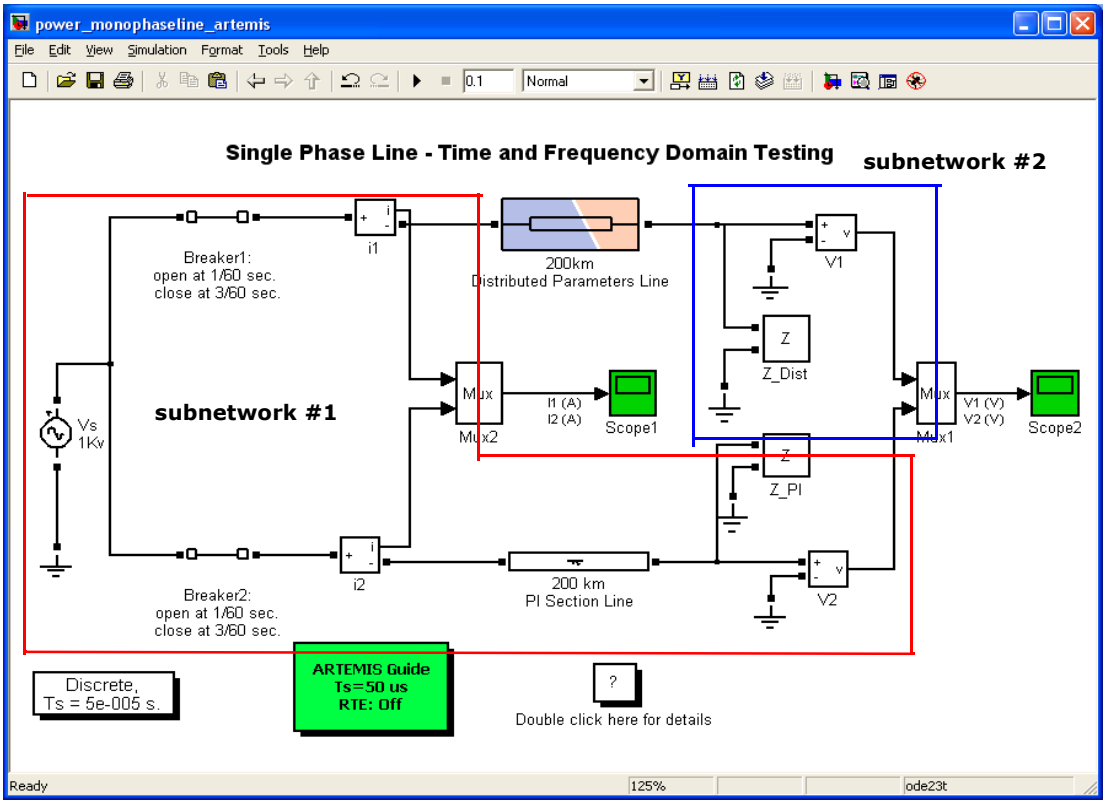
The example shows how to use the ARTEMIS distributed parameters line to decouple an electrical network into two distinct subnetworks and consenquently to optimize the time to simulate the system in real-time. This property also allows ARTEMIS to simulate systems that contains more switching elements and consequently more complex systems.

Note that the procedure shown below can also be apply to ARTEMIS Stubline block to decouple subnetworks and optimize real-time simulation.

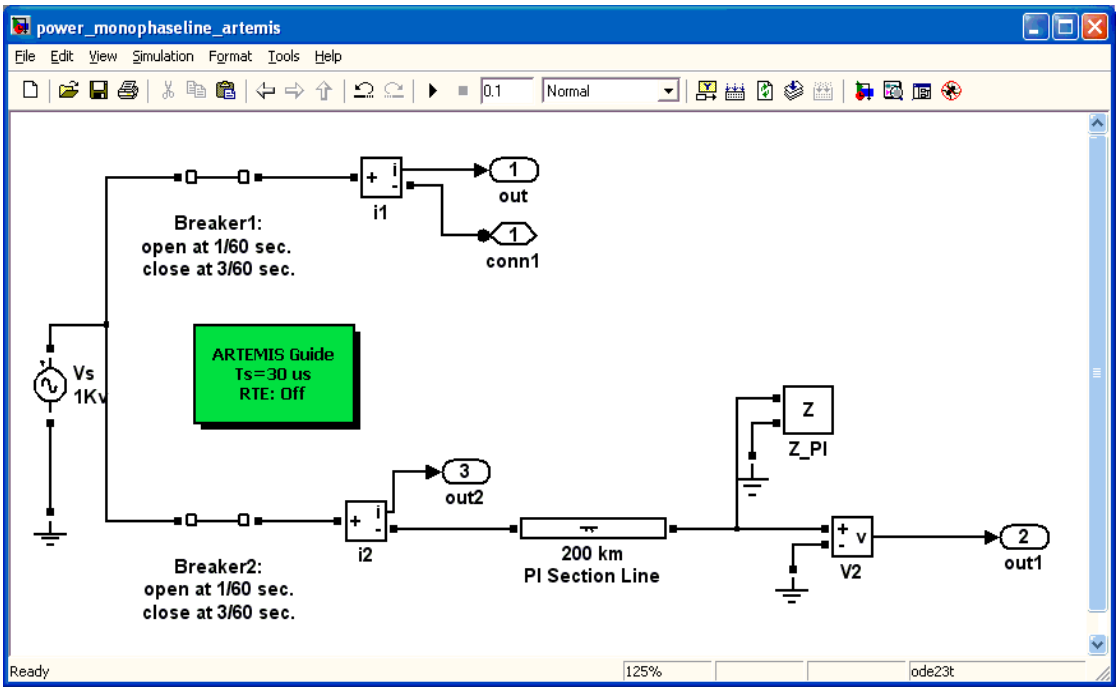
- Open the SPS demo power_monophaseline model by typing the following command in the command prompt of Matlab: power_monophaseline;
- To become familiar with the example, consult the help and perform simulation and check the results. The next steps will modify the demo to use the ARTEMIS solver instead of the normal SPS solver.
- Drag an ARTEMiS Guide block from the ARTEMiS library into the model and set it sample time to 50e-6 seconds.
- Set the SPS PowerGUI block to <Discrete> mode with a sample time equal to ARTEMiS
- Change the Distributed Parameter Line line block of SPS to the ARTEMIS block and copy the original line parameters in the ARTEMis Line model. Optionally, one can use the opReplaceSpsBlocks function. At the MATLAB prompt type: opReplaceSpsBlocks('power_monophaseline', 'ReplaceSpsBlocks');
- The model must be similar to the following figure. Save the model under the following name : power_monophaseline_artemis.mdl.



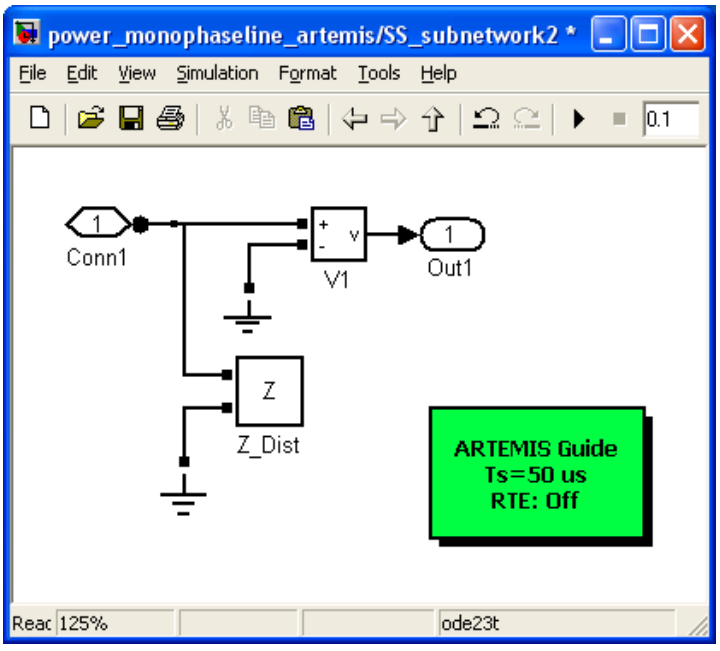
- Simulate the model and analyse the results. You will see that the results are similar to the original model.



- The next steps will show you how to run the model on a cluster of PCs running RT-LAB. The general idea is to benefit from the intrinsic delay of the transmission line to split the model into subnetworks. The mathematical model of the distributed parameters line of ARTEMIS, contrary to the SPS model, allows distribution of the line onto two different CPUs. This property also allows ARTEMIS to simulate systems that contains more switching elements and consequently more complex systems.
- Select all blocks located in the subnetwork 1 in the figure above and press Ctrl-G to create a new subsystem.
- Move the ARTEMIS block inside the subsystem.
- Rename this subsystem to SM_Subnetwork_1. The following figure displays the content of the SS_Subnetwork_1 subsystem.

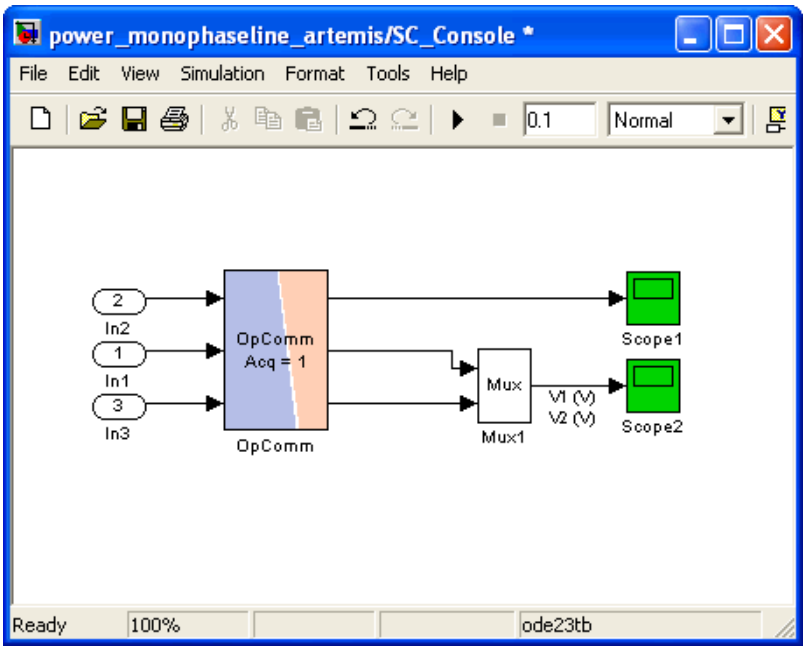


- Select all blocks located in the subnetwork 2 and press Ctrl-G to create a new subsystem.
- Add a ARTEMiS Guide block inside the subsystem.
- Rename this subsystem to SS_Subnetwork_2. The following figure illustrates the content of the SS_Subnetwork_2 subsystem.

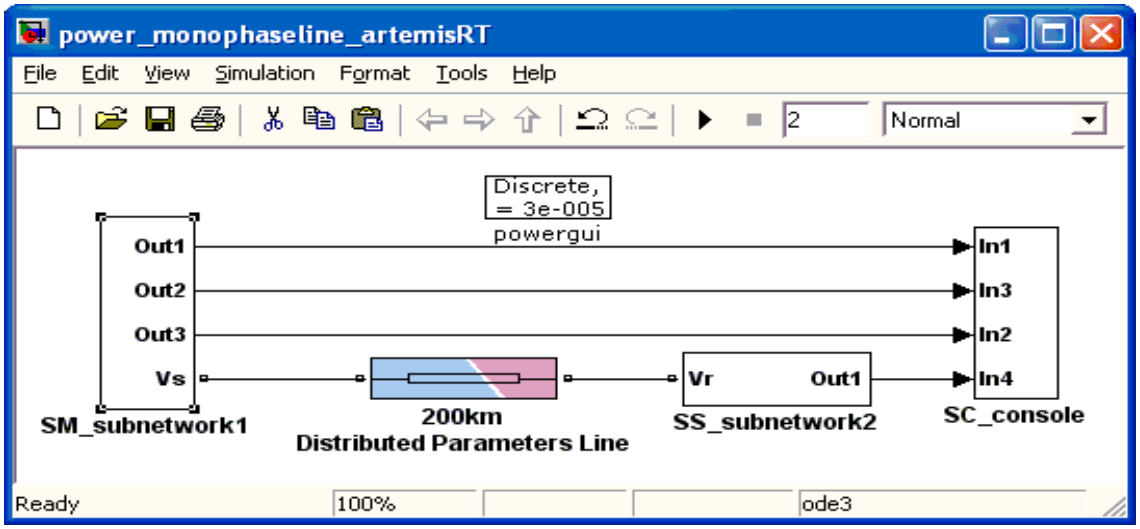


- Select the 3 remaining blocks, normally the two scopes blocks and the Mux1 block and press Ctrl-G to create a new subsystem.
- Rename this subsystem to SC_Console.

- Add the RT-LAB opcomm block between the inports blocks and the content of the subsystem. Don't forget to set the number of inports of the opcomm blocks to 3. Refer to the RT-LAB user guide for more help.
- The following figure illustrates the content of the SC_Console subsystem after the modifications described above have been made.



- Modify the solver parameters of the model; select one of the fixed-step solver, like ode3 for example, and change the fixed-step size to 50e-6.
- Organize the top level blocks according to the following figure. IMPORTANT: the powerGUI block must be at the top level.



- Save your model.
- Your model is now ready to be compiled with RT-LAB. Refer to the RT-LAB User Guide for more help. If your have set the sample times of your model with a variable set in the workspace(ex: Ts), you should set the model initialization function with <Ts=50e-6;> in File->Model Properties->Callbacks->InitFcn

Limitations

Usage in RT-LAB as task decoupling elements

When used in RT-LAB to decouple and separate computational tasks on different cores/CPUs, the following connection restriction are applicable to the ARTEMIS distributed parameters line model:

1- The ARTEMIS distributed parameters line must be located on the top-level of the RT-LAB compatible Simulink model

2- Each ARTEMIS distributed parameters line outports can be connected only to SimPowerSystems component located *inside* RT-LAB top-level subsystem (names beginning with 'SS' or 'SM' prefixes)

3- No connection between ARTEMIS distributed parameters lines is allowed on the top-level. If such a connection is required, the ARTEMIS distributed parameters block connection lines must be first routed inside the subsystems individually and the connection between the ARTEMIS distributed parameters line ports can be made inside the subsystem.

Related Items

OpReplaceSpsBlocks, **ARTEMiS Guide**, **ARTEMiS Stubline**

References

[1] Dommel, H., "Digital Computer Solution of Electromagnetic Transients in Single and Multiple Networks". IEEE Transactions on Power Apparatus and Systems, Vol. PAS-88, No. 4, April, 1969.

Library

ARTEMiS

Block

The ARTEMiS-SSN Frequency Dependent Line block implements an N-phases distributed parameters transmission line model with frequency dependence of line parameters.

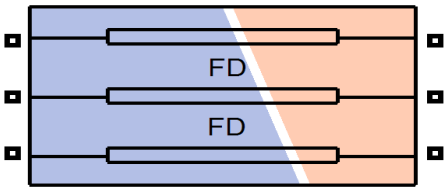


Figure 36:ARTEMiS-SSN Frequency Dependent Line block

Mask

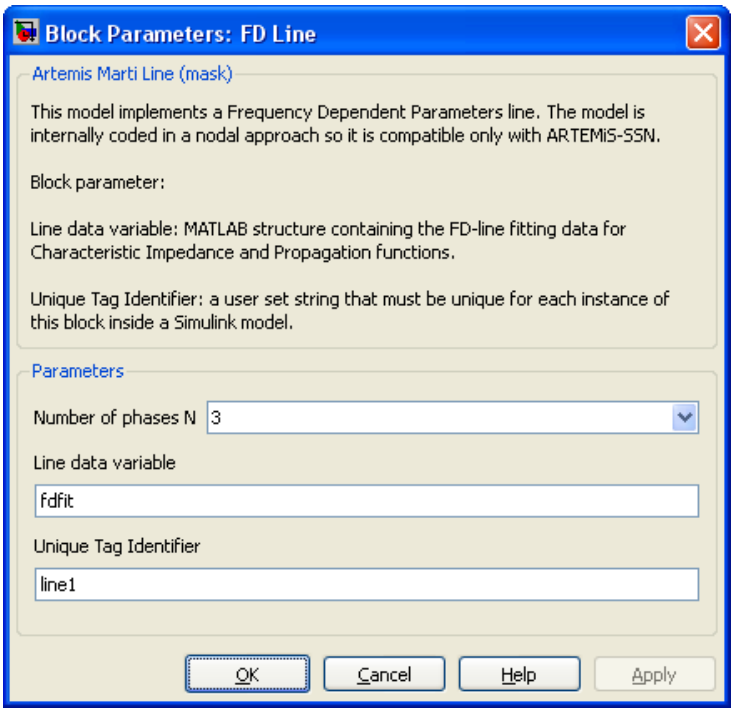

Block Parameters: FD Line
Artemis Marti Line (mask)
This model implements a Frequency Dependent Parameters line. The model is internally coded in a nodal approach so it is compatible only with ARTEMiS-SSN.
Block parameter:
Line data variable: MATLAB structure containing the FD-line fitting data for Characteristic Impedance and Propagation functions.
Unique Tag Identifier: a user set string that must be unique for each instance of this block inside a Simulink model.
Parameters
Number of phases N
3
Line data variable
fdfit
Unique Tag Identifier
line1
OK
Cancel
Help
Apply

Figure 37:Mask of the ARTEMiS-SSN Frequency Dependent Line block

Description

The ARTEMiS-SSN Frequency Dependent Line block implements an N-phases distributed parameters line model with frequency dependence of line parameters. The model is based on the Marti's model used by the Electromagnetic Transient Program (EMTP-RV) **[1][2]**.

This model is optimized for discrete real-time simulation and allows network decoupling. It also allows multi-CPU simulation on an RT-LAB simulator.

Parameters

Number of phases: the number of phase of the model (1-2-3-6)

Line data variable: the name of a MATLAB workspace variable containing the FD_line parameter. The variable is a structure containing the various parameter of the model.

>>fdfit =

Nph: [1x1 struct] .....number of phase
NpolY: [1x1 struct] ..... number of poles for Yc(s) (Yc=1/Zc)
Ypol: [1x1 struct]..... poles of Yc(s)
Yres: [1x1 struct] .....residues of Yc(s)
YDmat: [1x1 struct] ..... constant residues of Yc(s)
NpolH: [1x1 struct]..... number of poles of H(s)
Hpol: [1x1 struct].....poles of H(s) (propagation function)
Hres: [1x1 struct] .....residue of H(s)
HDmat: [1x1 struct]..... constant residues of H(s)
taumin: [1x1 struct] .....minimum propagation delays
Ti: [1x1 struct]..... current transformation matrix
Tv: [1x1 struct] .....voltage transformation matrix

And each component being itsefl a structure with Data and Name parts. For example:
>> fdfit.NpolY

Data: [3x1 double]
Name: 'Number of poles for each mode in Ycm'

The document untitled ***'Obtaining FD-line model parameters from EMTP-RV'*** explains how to get these parameters from the fitting routines of EMTP-RV.

Unique Tag Identifier: a user set string that must be unique for each instance of this block inside a Simulink model. (Note: in future releases, this parameters will be set automatically and will not be visible from the user)

Inputs

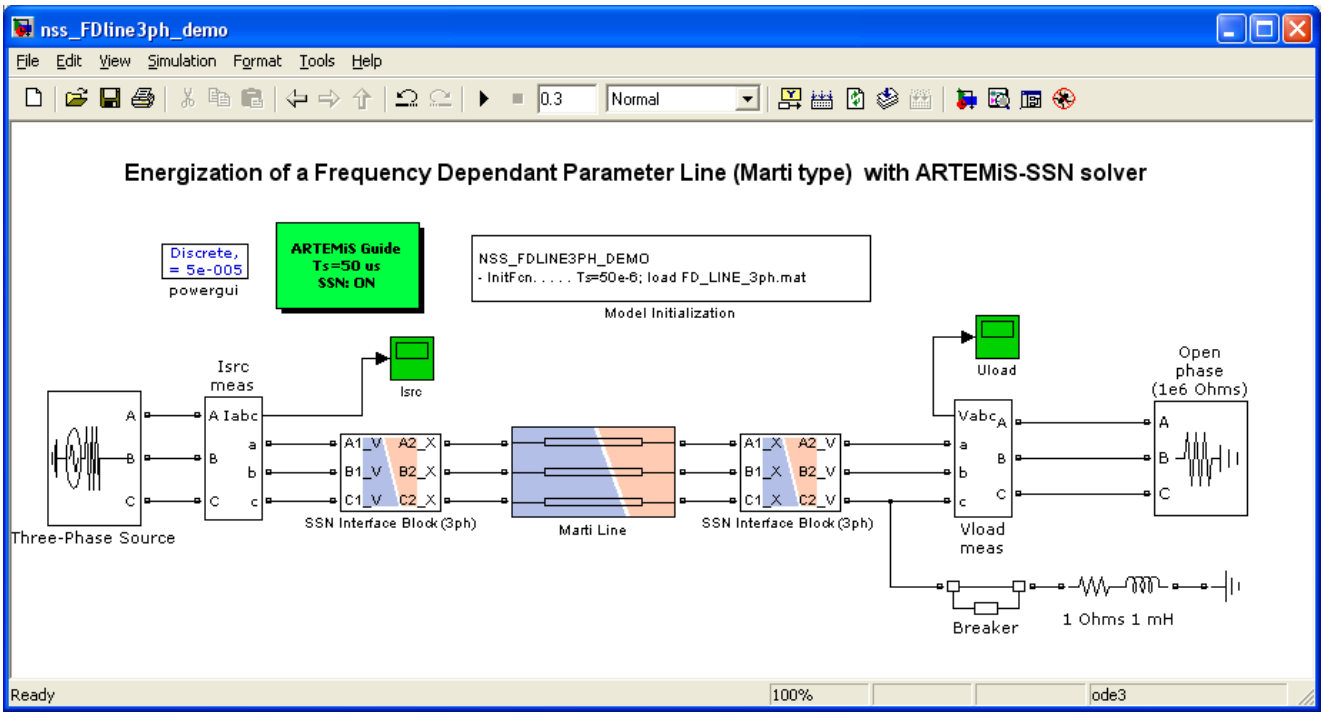
N-Phases voltage-current signals

Outputs

N-Phases delayed voltage-current signals.

Example

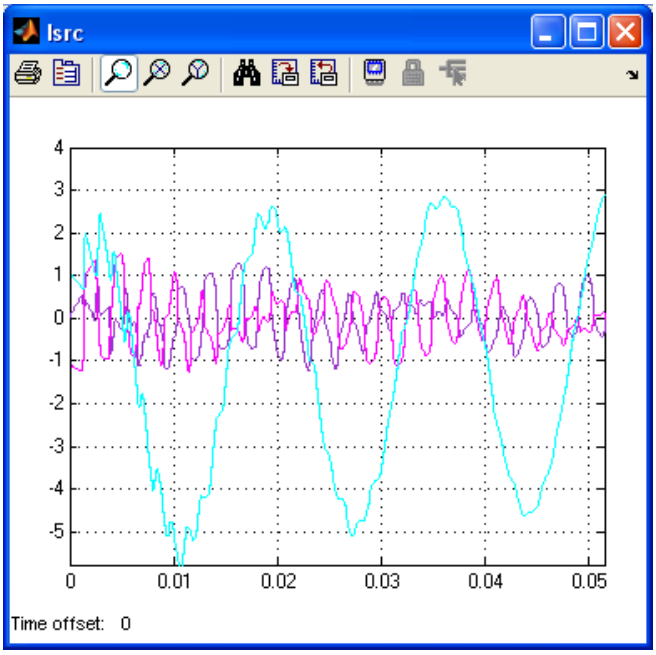
Offline usage example



The FD-line model interface with and only with the SSN method. The reason for this is that the FD-line model is internal coded with the nodal approach.

To make this interface, the FD-line model must be used in conjunction with SSN Nodal Interface Blocks (NIB) with the X-type interface chosen in the direction of the FD-line. The NIB can connect to other SSN groups of either V- I- or X-type.

The curve below shows the source energization current while phase C is connected to the 1Ω-1mH single phase load.



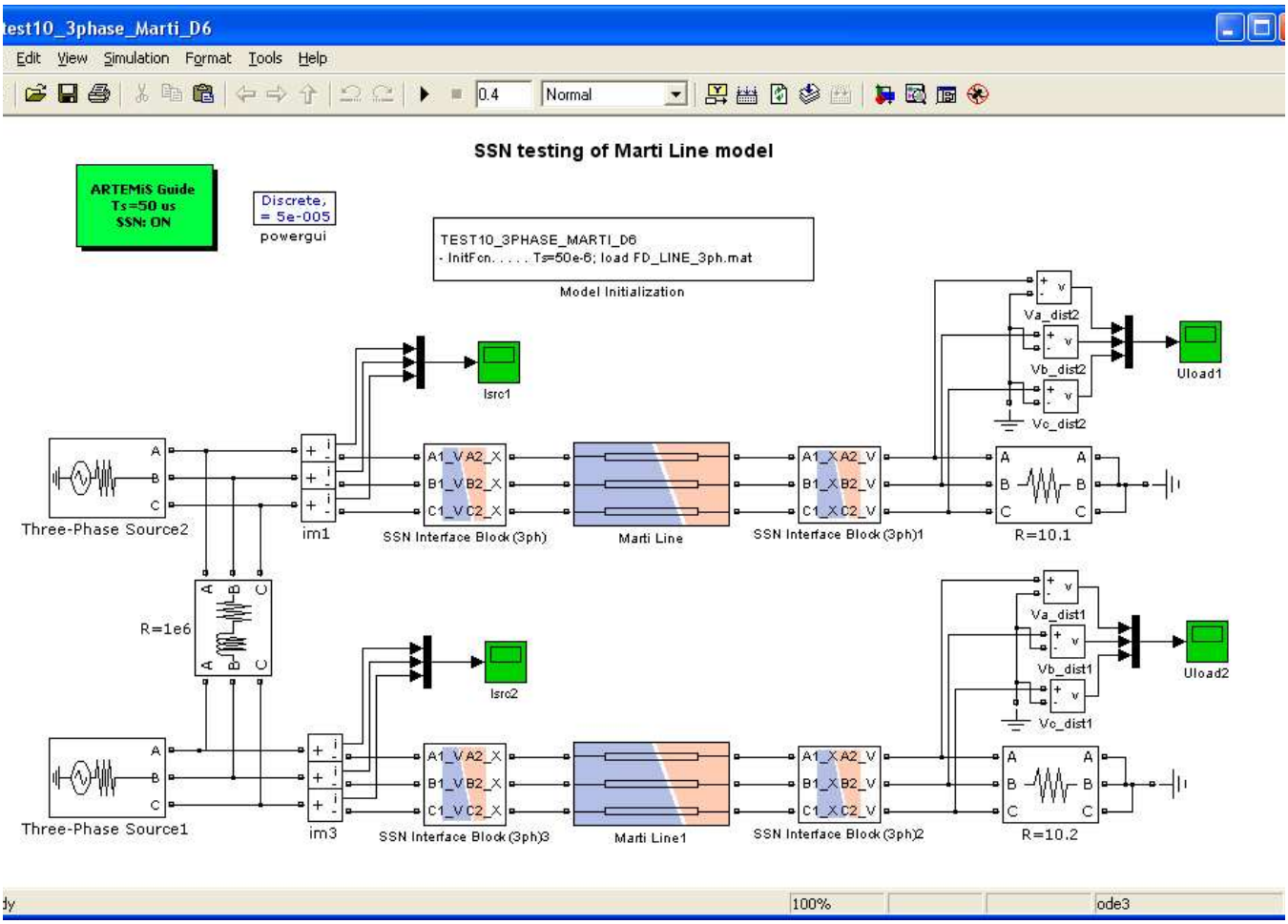
Real-time example

The distributed configuration of RT-LAB allows for complex models to be distributed over a cluster of PCs running in parallel. However, electrical circuit cannot be easily distributed over a multiple cores and/or cluster of PCs without changing the dynamic behaviors of the system.

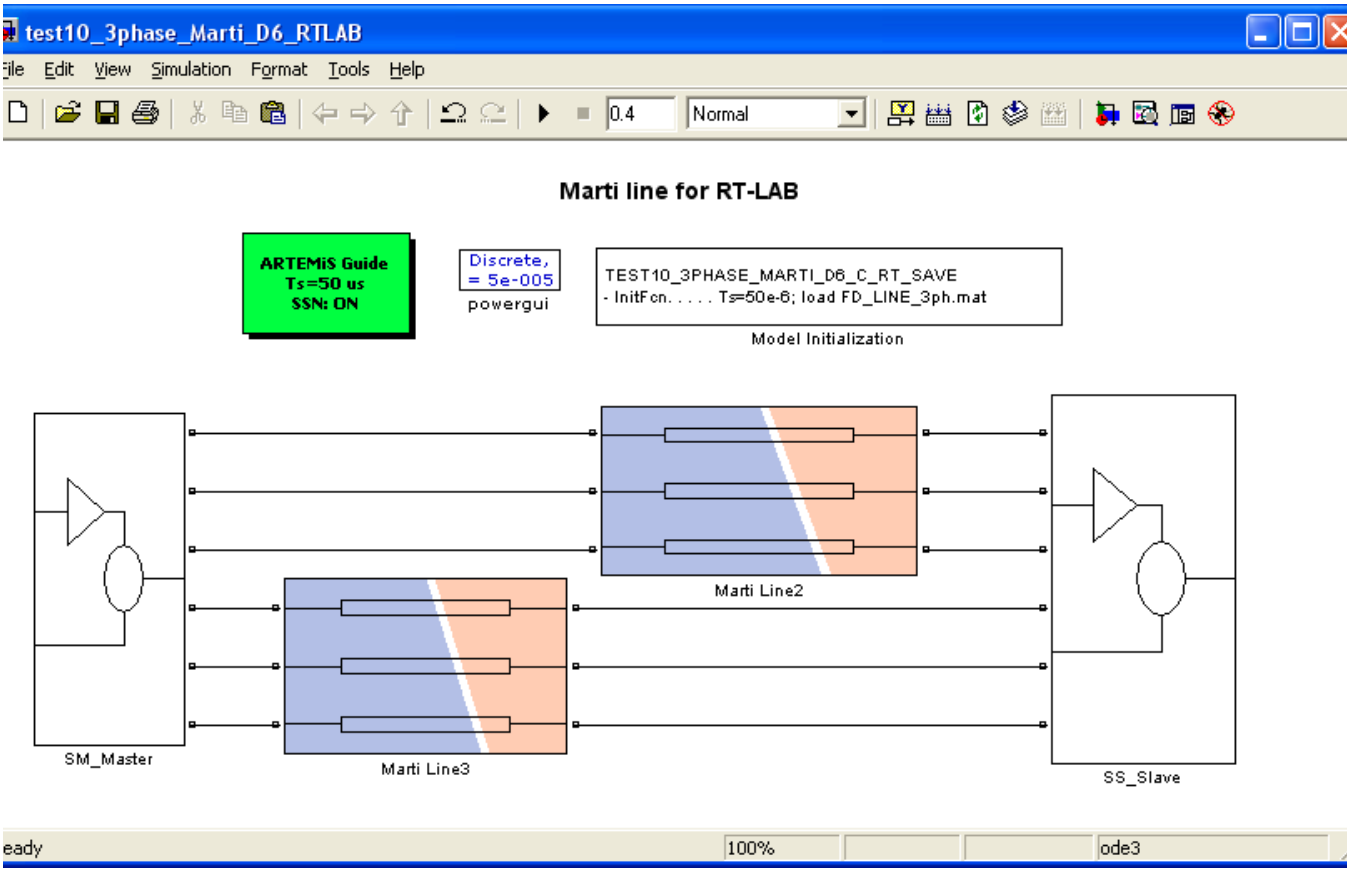
ARTEMiS lines (FD-line, Distributed Parameters Lines and Stublines) can be used to make the parallel simulation of an electric circuit. ARTEMiS used the intrinsic delay of the line to split the circuit without affecting the dynamic property of the system. See the **ARTEMiS Distributed Parameter Line** documentation for a complete example of the usage of ARTEMiS line models in the RT-LAB framework.

For real-time simulation the model had to be prepare according to RT-LAB conventions (SM_ SS_ top-level Simulink groups for example).

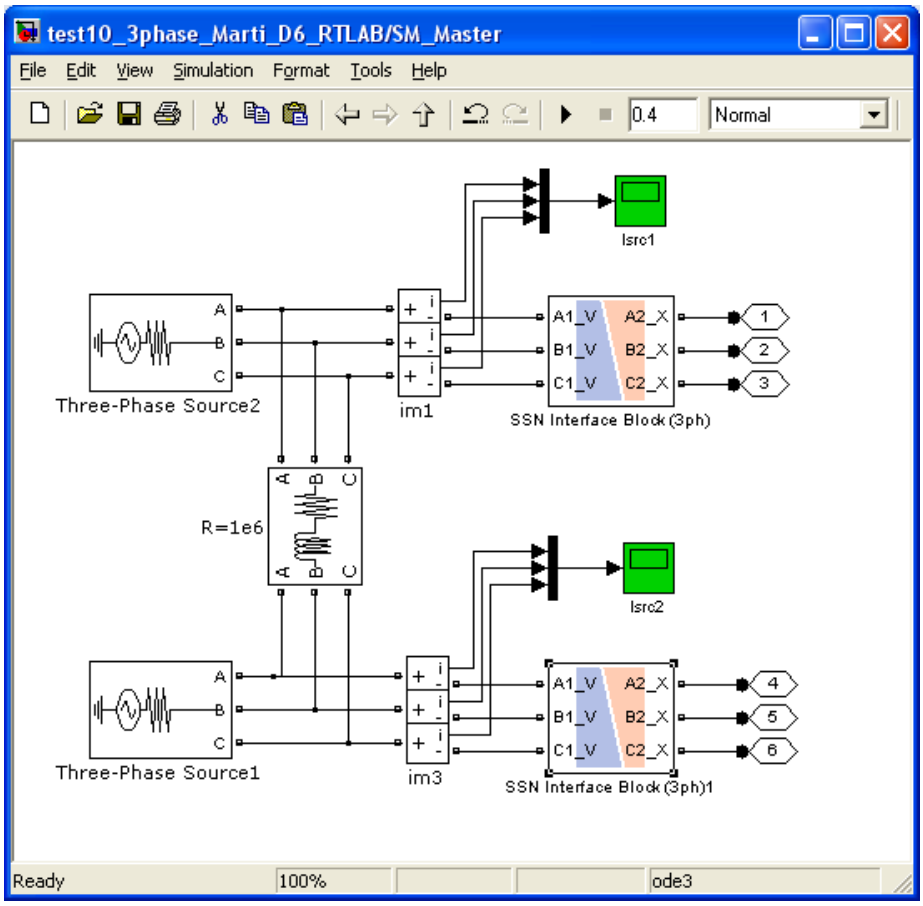
The model below contains 2 FD-line models connecting some source and loads.



The top-level separated model for RT-LAB will have the ARTEMiS-SSN Frequency Dependent Line model stay at the top-level of the diagram as shown below



And with the NIB block inside the SM_Master and SS_Slave subsystems like depicted below:



Compilation of this model in RT-LAB will results in two independent tasks (SM_Master and SS_Slave) interconnected by the 2 FD-line which will transmit their propagation voltage and currents between the two subsystems.

Characteristics and Limitations

Usage of the FD-line model in RT-LAB as task decoupling elements

When used in RT-LAB to decouple and separate computational tasks on different cores/CPUs, the following connection restriction are applicable to the ARTEMiS distributed parameters line model:

1- The ARTEMiS-SSN Frequency Dependent Line must be located on the top-level of the RT-LAB compatible Simulink model

2- Each ARTEMiS-SSN Frequency Dependent Line outports can be connected only to SimPowerSystems component located *inside* RT-LAB top-level subsystem (names beginning with 'SS' or 'SM' prefixes)

3- No connection between ARTEMiS-SSN Frequency Dependent Lines is allowed on the top-level. If such a connection is required, the ARTEMiS-SSN Frequency Dependent Line block connection lines must be first routed inside the subsystems individually and the connection between the ARTEMiS-SSN Frequency Dependent Line ports can be made inside the subsystem.

SSN solver in the ARTEMiS GUIde block

The SSN solver of the ARTEMiS GUIde block must be 'Trapezoidal' when using a ARTEMiS-SSN Frequency Dependent Line block. This is because the Trapezoidal solver is used internally by the ARTEMiS-SSN Frequency Dependent Line block.

Initialisation

The ARTEMiS-SSN Frequency Dependent Line block does not initialize in steady-state so unexpected transients at the beginning of the simulation may occur.

Direct Feedthrough	No
Discrete sample time	Yes, defined in the ARTEMiS guide block.
XHP support	Yes
Work offline	Yes

Related Items

OpReplaceSpsBlocks, ARTEMiS Guide, ARTEMiS Stubline, ARTEMIS Distributed Parameters Line, ARTEMiS-SSN Nodal interface Blocks.

References

[2] J.R. Marti, "Accurate Modelling of Frequency-Dependent Transmission Lines in Electromagnetic Transient Simulations", IEEE Trans. on Power App. and Systems, Vol. PAS-101, No. 1,January 1982, pp. 147-155.

[3] C. Dufour, H. Le-Huy, J.-C. Soumagne, A. El Hakimi, "Real-Time Simulation of Power Transmission Lines using Marti Model with Optimal Fitting on Dual-DSP Card", IEEE Trans. on Power Delivery, Vol.11, No.1, Jan. 1996, pp. 412-419.

Library

ARTEMIS

Block

The ARTEMiS Stubline block implements an N-phase distributed parameters transmission line model with exactly one time step propagation delay. It is optimized for real-time simulation.

The ARTEMiS Stubline block permits the decoupling of state-space system equations of networks on both sides of the stubline.

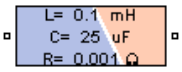


Figure 38:ARTEMiS Stubline block

Mask

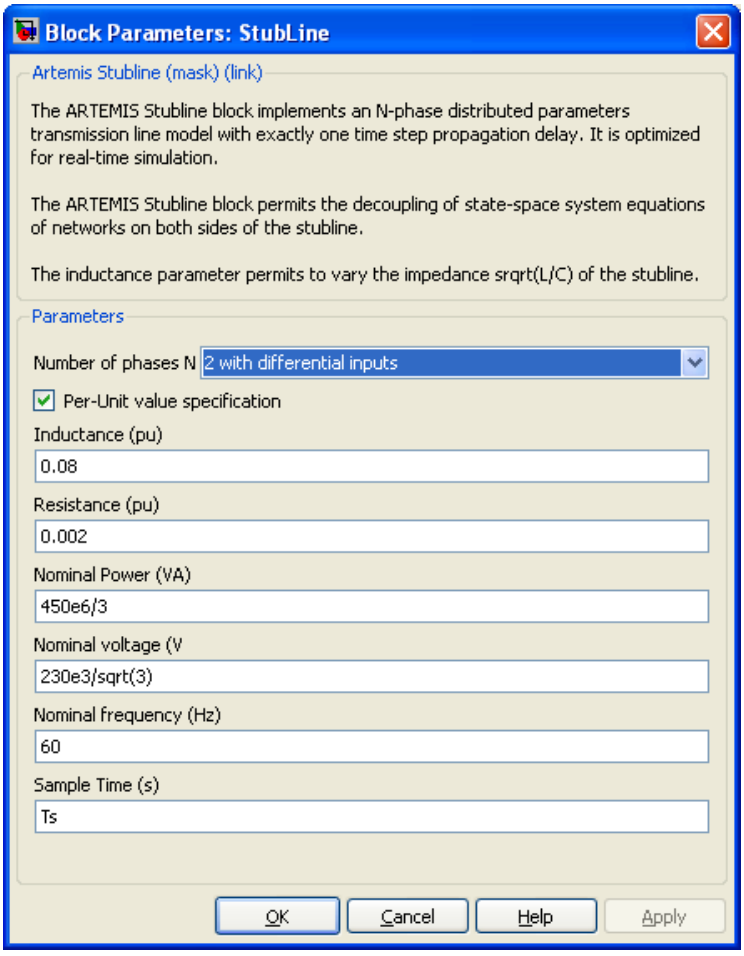

Block Parameters: StubLine
Artemis Stubline (mask) (link)
The ARTEMIS Stubline block implements an N-phase distributed parameters transmission line model with exactly one time step propagation delay. It is optimized for real-time simulation.
The ARTEMIS Stubline block permits the decoupling of state-space system equations of networks on both sides of the stubline.
The inductance parameter permits to vary the impedance srqrt(L/C) of the stubline.
Parameters
Number of phases N
2 with differential inputs
Per-Unit value specification
Inductance (pu)
0.08
Resistance (pu)
0.002
Nominal Power (VA)
450e6/3
Nominal voltage (V
230e3/sqrt(3)
Nominal frequency (Hz)
60
Sample Time (s)
Ts
OK
Cancel
Help
Apply

Figure 39:Mask of the ARTEMIS Stubline block

Description

The ARTEMiS Stubline block implements an N-phase distributed parameters transmission line model with exactly one time step propagation delay. The model is based on the Bergeron's travelling wave method used by the Electromagnetic Transient Program (EMTP) **[1]**. This block is similar to the SPS distributed parameters line block but is optimized for discrete real-time simulation and allows network decoupling. It also allows multi-CPU simulation on an RT-LAB simulator.

Refer to the SPS Distributed Parameter Line block Reference page for more details on the mathematical model of the distributed parameters line.

Network decoupling
One of the main advantage of the ARTEMiS line blocks (Distributed parameters lines and Stublines), by opposition to the SPS lines, is the decoupling of the electric circuit into smaller subnetworks. This important property allows ARTEMiS to simulate, in real-time, circuit with more switching elements.

SPS and ARTEMiS solve electric circuits using the common state-space method. One of the main limitation of this method is related to the switch elements. When an event occurs that changes the topology of the circuit (or change the state of a switch), SPS and ARTEMiS need to compute a new state-space matrix. This calculation causes a non acceptable overhead when simulating a circuit in real-time.

To solve this problem, ARTEMiS stores the state-space matrices of a given set of topologies, normally the steady-state topologies, in cached memory and uses them when necessary without having to recalcule the matrices. However, the number of matrices required to cover all topologies of the system depends on the number of switch elements. When a circuit contains a lot of switch elements, the number of required topologies is high and it is not possible to store all matrices in cached memory because of the size of the matrices.

The decoupling property of the line allows ARTEMiS to divide the state-space system in two different state-space systems and reduce the total size of the state-space matrices in memory. It also reduces the maximum number of topologies by an important factor.

RT-LAB simulation using a cluster of PCs
The distributed configuration of RT-LAB allows for complex models to be distributed over a cluster of PCs running in parallel. The target nodes in the cluster communicate between each other with low latency protocols such as shared memory, FireWire, SignalWire or InfiniBand, fast enough to provide reliable communication for real-time applications.

However, electrical circuit cannot be easily distributed over a cluster of PCs without changing the dynamic behaviors of the system. The communication delays degrade the computation.

ARTEMiS lines (Distributed Parameters Lines and Stublines) can be used to distribute a circuit over a cluster of PCs. ARTEMiS used the intrinsic delay of the line to split the circuit without affecting the dynamic property of the system. Moreover, SPS and ARTEMiS use physical modelling lines and connectors to model the circuit. This type of signals cannot be used by RT-LAB to communicate signals between subsystems, because the RT-LAB opcomm block only supports basic Simulink signals. The only exception to this rule are the ARTEMiS **Distributed Parameters Line** block and the ARTEMiS **Stubline** block. RT-LAB allows the insertion of a line block at the root level of the block diagram and the connection of the

physical modelling ports of the block to the real-time subsystems. Also note that the physical modelling signals and ports do not have to pass through the opcomm block.

Parameters

Number of phases N: Specifies the number of phases, N, of the model. The block dynamically changes according to the number of phases that you specify. When you apply the parameters or close the dialog box, the number of inputs and outputs is updated. Available number are 1 to 6 and '2 (differential input)'. This last option is useful when using ARTEMiS Stubline in case where it do not have to be refered to ground like in stubline transformer applications.

Per-Unit value specification: Specify if the resistance and inductance value are specified in per-unit or not.

Resistance per unit length: The resistance R per unit length, in ohms/km or pu..

Inductance per unit length: The inductance L per unit length, in henries/km (H/km) or pu.

Nominal power (VA): Nominal power base (for per-unit values only).

Nominal voltage(V): Nominal voltage base (for per-unit values only).

Nominal frequency (Hz): Nominal frequency base (for per-unit values only).

Sample Time: The block sample time, in second (s).

Inputs

N-Phases voltage-current physical domain connection.

Outputs

N-Phases delayed voltage-current physical domain connection.

Characteristics and Limitations

The ARTEMiS Stubline block does not initialize in steady-state so unexpected transients at the beginning of the simulation may occur.

Direct Feedthrough	No
Discrete sample time	Yes, defined in the ARTEMiS guide block.
XHP support	Yes
Work offline	Yes

Example

This section provides an example on how to build a 3-phase stubline transformer. The stubline transformer will exhibit a decoupling delay between the primary and secondary sides suitable for distributed simulation real-time simulation of large systems. Such a transformer could be used to decouple HVDC system equations at the rectifier/inverter

station transformers and compute each equations in parallel on different CPUs or cores. The model is part of the ARTEMiS demos and is named artemis_Transfo_Stubline (.mdl).

In the example, we construct a stubline-based 3-phase transformer from an original SimPowerSystems transformer and compare the no-load and short-circuit responses. The principle used to build the stubline transformer is to 'move' the secondary windings leakage inductance and resistance in stublines put in series with the windings themself. This is done using single-phase transformers first, then adjusting the per-unit stubline parameters and finally to make the Y ou Delta connections after the stubline.

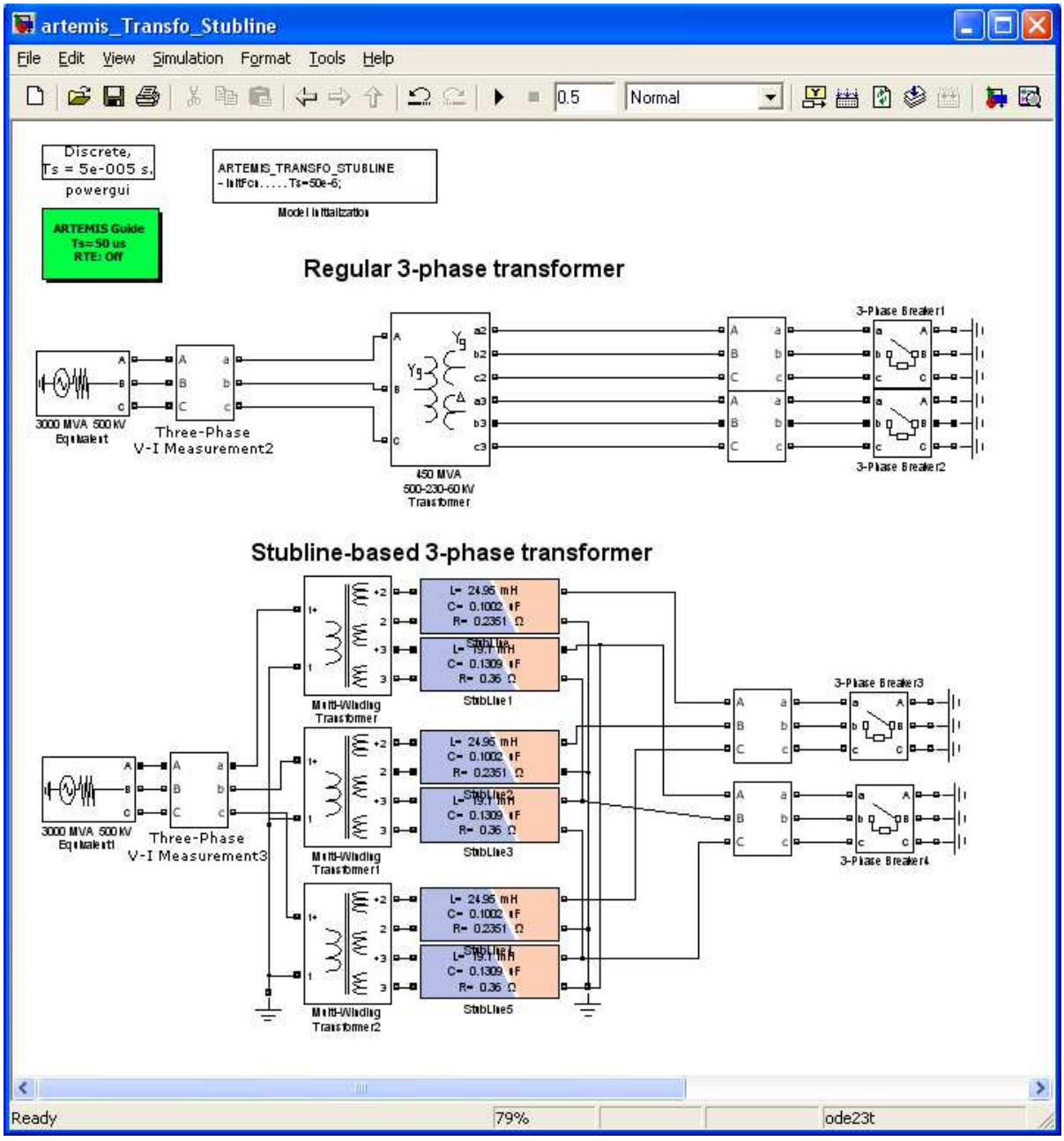


Figure 3: Model of a stubline transformer

The example uses a SPS 3-phase transformer with the following parameters:

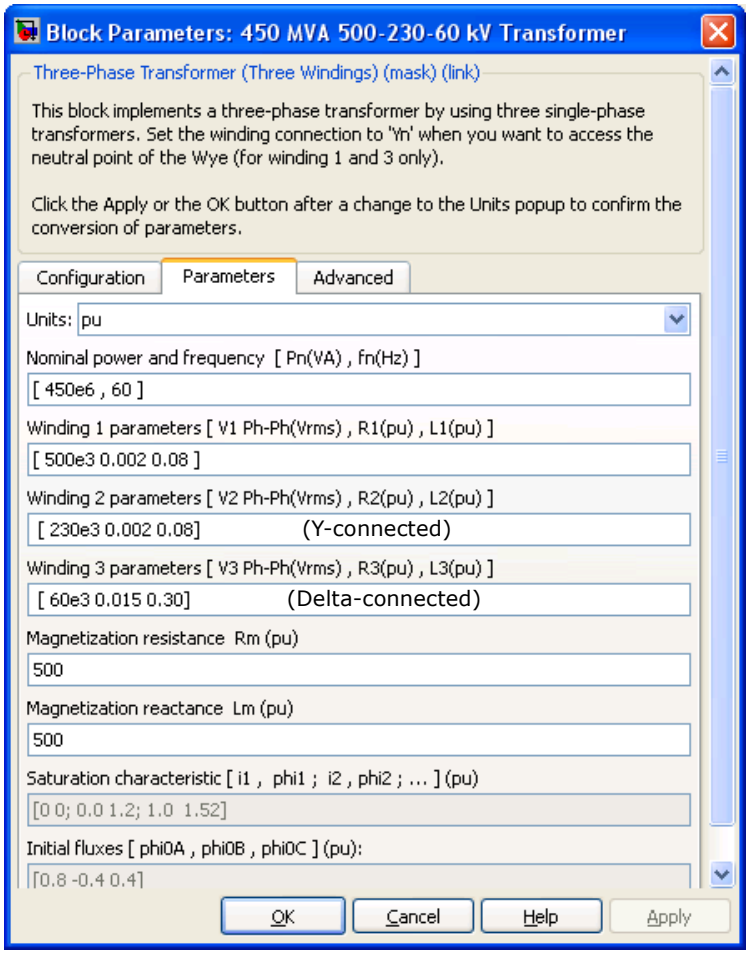

Block Parameters: 450 MVA 500-230-60 kV Transformer
Three-Phase Transformer (Three Windings) (mask) (link)
This block implements a three-phase transformer by using three single-phase transformers. Set the winding connection to 'Yn' when you want to access the neutral point of the Wye (for winding 1 and 3 only).
Click the Apply or the OK button after a change to the Units popup to confirm the conversion of parameters.
Configuration
Parameters
Advanced
Units: pu
Nominal power and frequency [Pn(VA) , fn(Hz)]
[450e6 , 60]
Winding 1 parameters [V1 Ph-Ph(Vrms) , R1(pu) , L1(pu)]
[500e3 0.002 0.08]
Winding 2 parameters [V2 Ph-Ph(Vrms) , R2(pu) , L2(pu)]
[230e3 0.002 0.08]
(Y-connected)
Winding 3 parameters [V3 Ph-Ph(Vrms) , R3(pu) , L3(pu)]
[60e3 0.015 0.30]
(Delta-connected)
Magnetization resistance Rm (pu)
500
Magnetization reactance Lm (pu)
500
Saturation characteristic [i1 , phi1 ; i2 , phi2 ; ...] (pu)
[0 0; 0.0 1.2; 1.0 1.52]
Initial fluxes [phi0A , phi0B , phi0C] (pu):
[0.8 -0.4 0.4]
OK
Cancel
Help
Apply

Figure 4: Three-phase transformer parameters

We will build the stubline 3-phase transformer using single-phase transformer using pu units. Since we will also use pu-based differential stubline (a stubline with no built-in ground referentials), appropriate single-phase per-unit bases have to be found. First, the total 3-phase nominal power has to be divided by 3 when configuring single-phase transformer inside. Secondly, the 3-phase winding voltage takes into account the connection type (Y or Delta) in the voltage specification while single-phase transformer has no such thing. Third, the R-L pu specification of a 3-phase transformer are specified as 'Y-connection equivalent values'.

In the final, the resulting single phase transformer therefore has the following parameters:

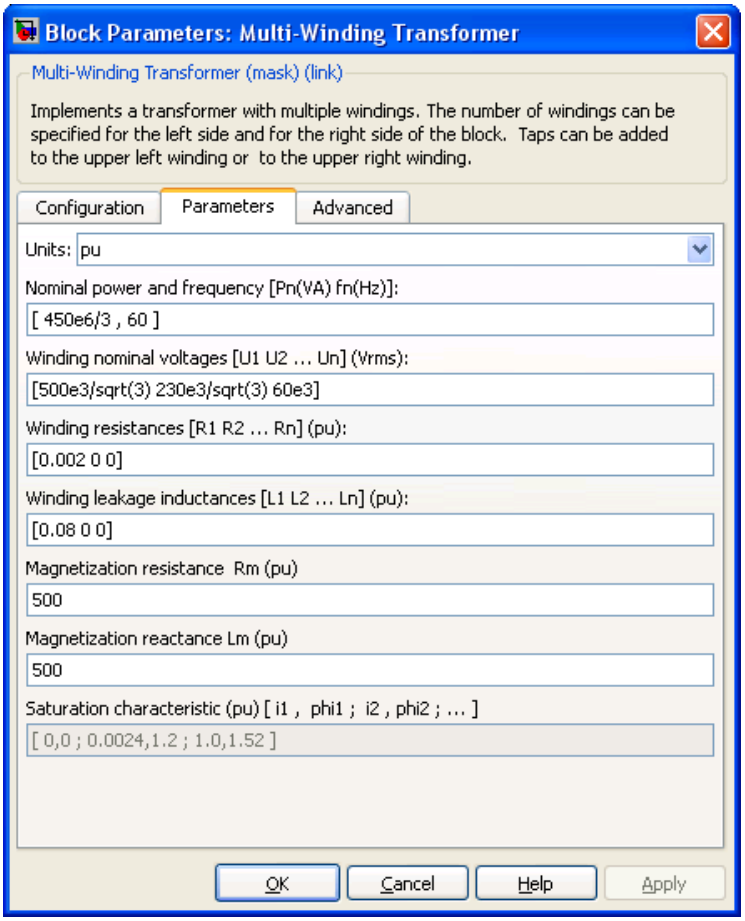

Block Parameters: Multi-Winding Transformer
Multi-Winding Transformer (mask) (link)
Implements a transformer with multiple windings. The number of windings can be specified for the left side and for the right side of the block. Taps can be added to the upper left winding or to the upper right winding.
Configuration
Parameters
Advanced
Units: pu
Nominal power and frequency [Pn(VA) fn(Hz)]:
[450e6/3 , 60]
Winding nominal voltages [U1 U2 ... Un] (Vrms):
[500e3/sqrt(3) 230e3/sqrt(3) 60e3]
Winding resistances [R1 R2 ... Rn] (pu):
[0.002 0 0]
Winding leakage inductances [L1 L2 ... Ln] (pu):
[0.08 0 0]
Magnetization resistance Rm (pu)
500
Magnetization reactance Lm (pu)
500
Saturation characteristic (pu) [i1 , phi1 ; i2 , phi2 ; ...]
[0,0 ; 0.0024,1.2 ; 1.0,1.52]
OK
Cancel
Help
Apply

Figure 5: Single phase transformer parameters (with null secondary R-L parameters)

Note that the single-phase transformer winding that are Y connected have their voltage ratio cut by a sqrt(3) factor. Also note the nominal power that is cut by a factor 3. The ARTEMiS Stubline put in the Y connection has the following parameters:

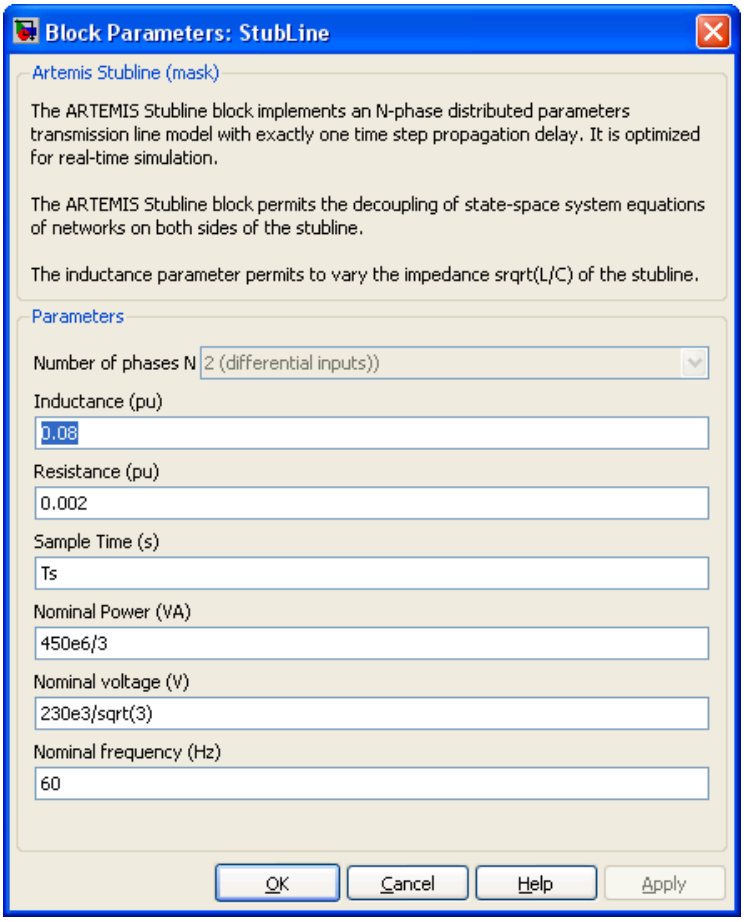

Block Parameters: StubLine
Artemis Stubline (mask)
The ARTEMIS Stubline block implements an N-phase distributed parameters transmission line model with exactly one time step propagation delay. It is optimized for real-time simulation.
The ARTEMIS Stubline block permits the decoupling of state-space system equations of networks on both sides of the stubline.
The inductance parameter permits to vary the impedance srqrt(L/C) of the stubline.
Parameters
Number of phases N
2 (differential inputs))
Inductance (pu)
0.08
Resistance (pu)
0.002
Sample Time (s)
Ts
Nominal Power (VA)
450e6/3
Nominal voltage (V)
230e3/sqrt(3)
Nominal frequency (Hz)
60
OK
Cancel
Help
Apply

Figure 6: ARTEMiS Stubline parameters (Y-connected windings)

while the ARTEMiS Stubline put in the Delta connection has the following parameters:

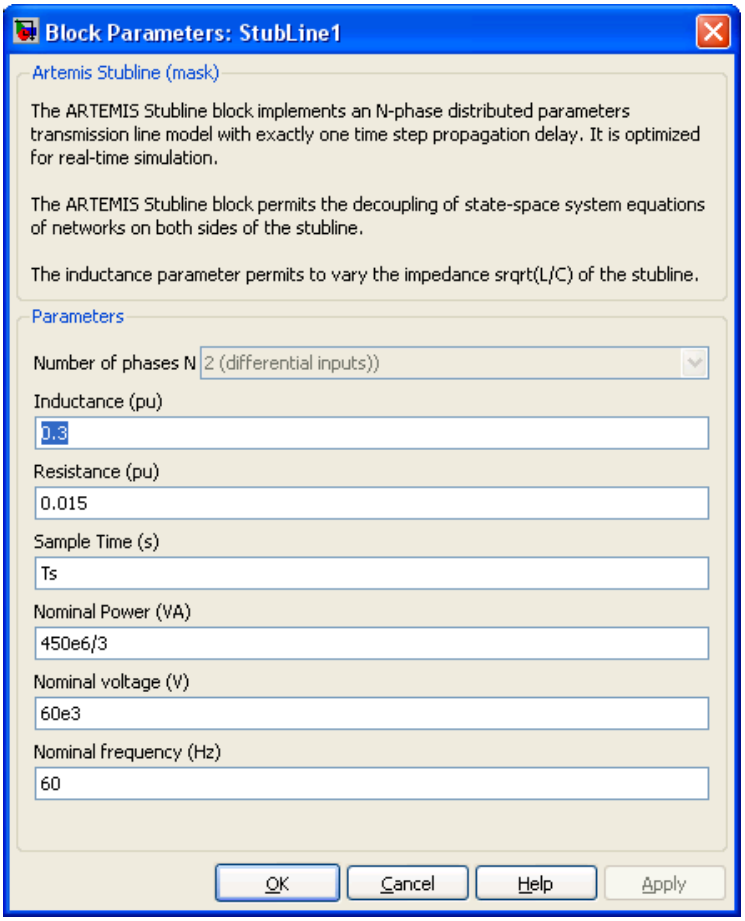

Block Parameters: StubLine1
Artemis Stubline (mask)
The ARTEMIS Stubline block implements an N-phase distributed parameters transmission line model with exactly one time step propagation delay. It is optimized for real-time simulation.
The ARTEMIS Stubline block permits the decoupling of state-space system equations of networks on both sides of the stubline.
The inductance parameter permits to vary the impedance srqrt(L/C) of the stubline.
Parameters
Number of phases N
2 (differential inputs))
Inductance (pu)
0.3
Resistance (pu)
0.015
Sample Time (s)
Ts
Nominal Power (VA)
450e6/3
Nominal voltage (V)
60e3
Nominal frequency (Hz)
60
OK
Cancel
Help
Apply

Figure 7: ARTEMiS Stubline parameters (Delta-connected windings)

Note that the bases used are consequent with the parameters of the single-pase transformer. The R-L per-unit values are the same than in the 3-phase transformer. Only the base voltage values differ depending on the connection type.

The design of such transformers is often tricky because of the possible errors in the base conversion. It is always advisable to compare the stubline model with a rererence for no-load and short-circuit cases to verify the correctness of the design. This is what is done in the example where we superpose the voltages and currents of the stubline transformer with a standard SPS model.

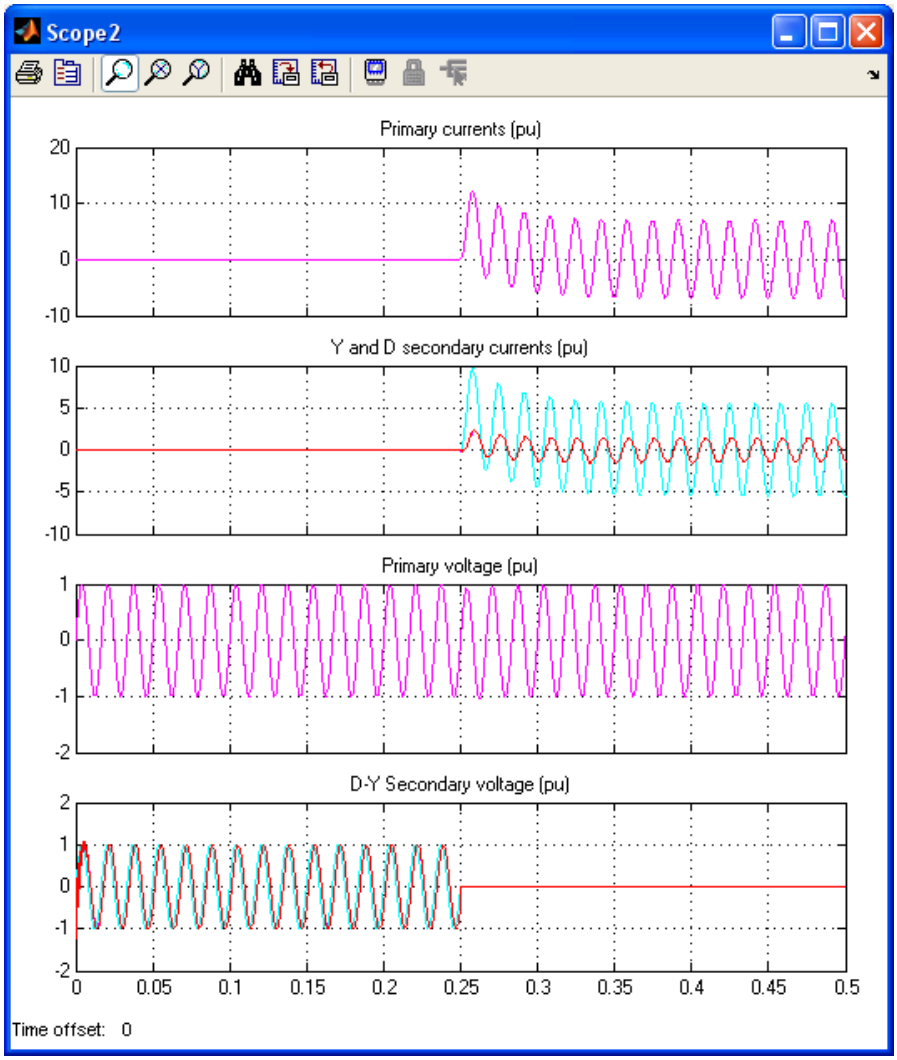


Figure 8: Comparison of stubline- and SPS- transformers values for no-load (before 0.25 sec.) and short-circuit (after 0.25 sec.)

Finally, this model can be simulated in several CPU if the model is separated in accordance to RT-LAB rules with the stublines used as inter-CPU decoupling elements placed on the top-level of the Simulink model.

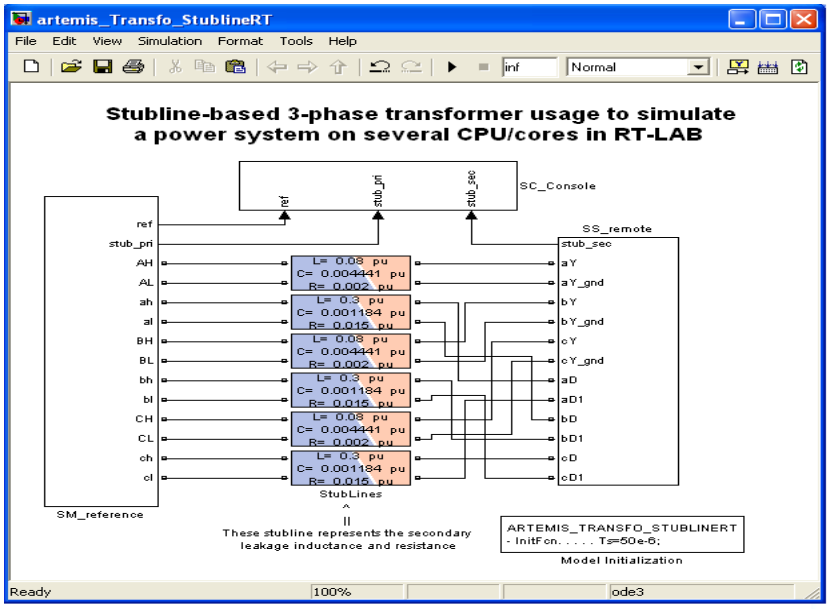


Figure 9: Stublines usage in RT-LAB to decouple compuational task on several cores/CPUs

See the artemis_Transfo_StublineRT.mdl demo for details on how to use the stublines to decouple and simulate such a model on several cores/CPUs in RT-LAB.

Limitations

Usage in RT-LAB as task decoupling elements

When used in RT-LAB to decouple and separate computational tasks on different cores/CPUs, the following connection restriction are applicable to the ARTEMiS Stubline model:

1- The ARTEMiS Stubline must be located on the top-level of the RT-LAB compatible Simulink model (as in Figure 9 for example)

2- Each ARTEMiS Stubline outports can be connected only to SimPowerSystems component located *inside* RT-LAB top-level subsystem (names beginning with 'SS' or 'SM' prefixes)

3- No connection between stublines is allowed on the top-level. If such a connection is required (ex: star-connection neutral point), the ARTEMiS Stubline lines must be first routed inside the subsystems individually and the connection between the ARTEMiS Stubline ports can be made inside the subsystem.

Related Items

OpReplaceSpsBlocks, **ARTEMiS Guide**, **ARTEMIS Distributed Parameters Line**

ARTEMiS Transformer with Switched Saturable Core

Library

ARTEMiS (Advanced Real-Time ElectroMagnetic Simulator)

Block

The ARTEMiS-Transformer with Switched Saturable Core implements a 3-phase saturable transformer in SimPowerSystems model using a switched saturable core method instead of the current injection with delay of the native SPS transformer models. This type of model is use to solve instability problems of the current injection methods with delay.

Available models are zigzag-Y , Y-Y, Y-D (±30 deg.), in PU and SI versions.

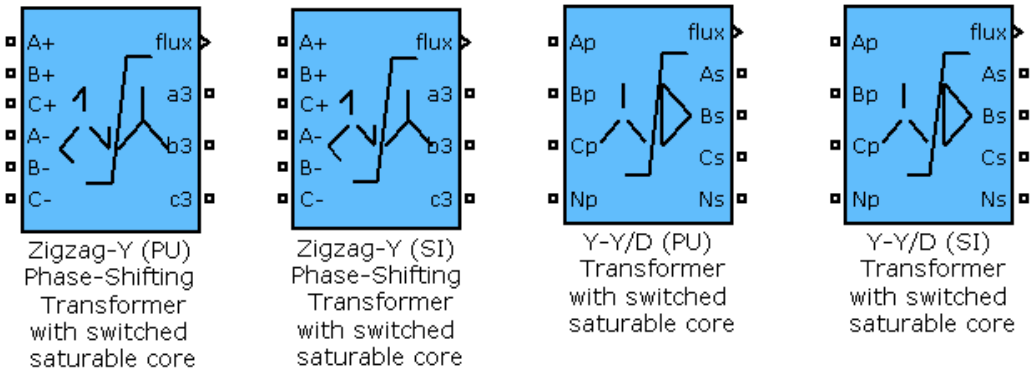


Figure 40:ARTEMiS Transformer with Switched saturable Core

Mask

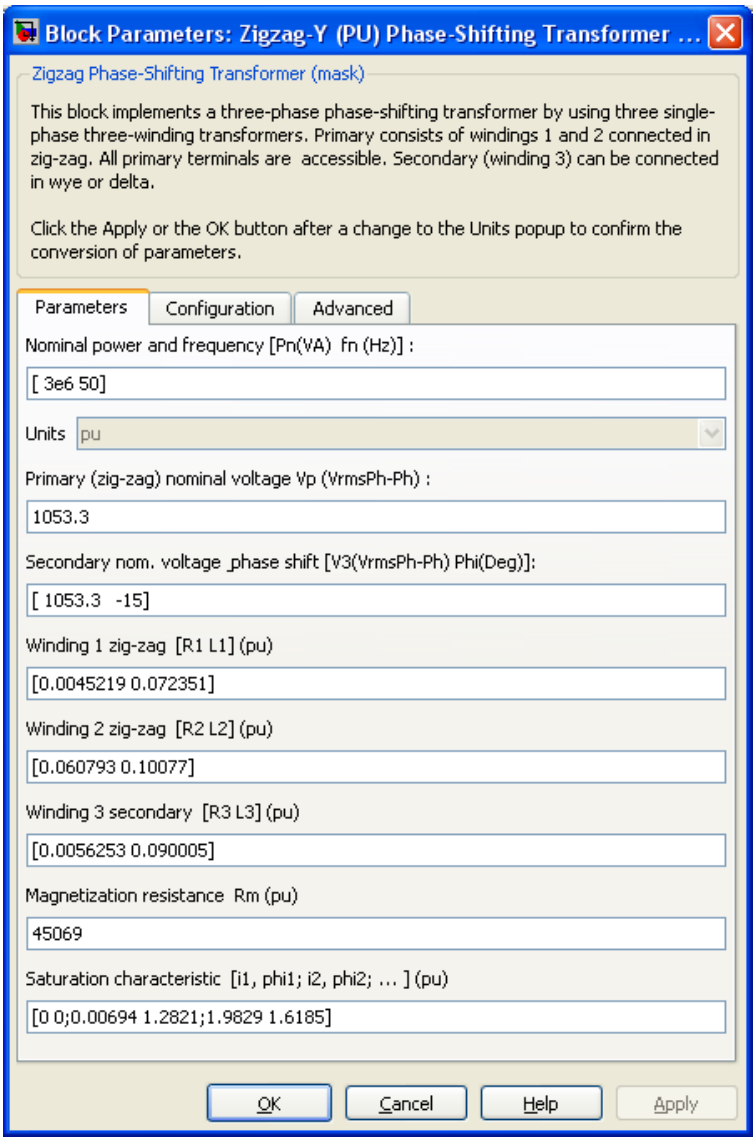

Block Parameters: Zigzag-Y (PU) Phase-Shifting Transformer ...
Zigzag Phase-Shifting Transformer (mask)
This block implements a three-phase phase-shifting transformer by using three single-phase three-winding transformers. Primary consists of windings 1 and 2 connected in zig-zag. All primary terminals are accessible. Secondary (winding 3) can be connected in wye or delta.
Click the Apply or the OK button after a change to the Units popup to confirm the conversion of parameters.
Parameters
Configuration
Advanced
Nominal power and frequency [Pn(VA) fn (Hz)] :
[3e6 50]
Units
pu
Primary (zig-zag) nominal voltage Vp (VrmsPh-Ph) :
1053.3
Secondary nom. voltage _phase shift [V3(VrmsPh-Ph) Phi(Deg)]:
[1053.3 -15]
Winding 1 zig-zag [R1 L1] (pu)
[0.0045219 0.072351]
Winding 2 zig-zag [R2 L2] (pu)
[0.060793 0.10077]
Winding 3 secondary [R3 L3] (pu)
[0.0056253 0.090005]
Magnetization resistance Rm (pu)
45069
Saturation characteristic [i1, phi1; i2, phi2; ...] (pu)
[0 0;0.00694 1.2821;1.9829 1.6185]
OK
Cancel
Help
Apply

Figure 41:Mask of the ARTEMiS Transformer with Switched saturable Core (zigzag-Y)

Description

The ARTEMiS-Transformer with Switched Saturable Core implements a 3-phase saturable transformer in SimPowerSystems model using a switched saturable core method instead of the current injection with delay of the native SPS transformer models. The model is to be used in conjunction with the ARTEMiS GUIde block.

The model is based on the SimPowerSystems transformer model for the linear part. The non-linear part, i.e. the saturation is modeled has a switched core inductance. In the linear region of operation, the first segment of the i=f(flux) characteristic is included in the ABCD state-space matrix and flux is monitored from there. Whenever the flux reach the 2nd (and last) segment of the i=f(flux) characteristic, a inductance is switched in parallel with the

linear one and simulation continues with the new configuration of the circuit caused by this switching action.

Parameters (zig-zag)

Units: Specify the units used (SI or PU) for Zigzag Phase-Shifting Transformer block. Two different blocks must be used for SI or PU units.

Nominal power and frequency: The nominal power rating, in volt-amperes (VA), and nominal frequency, in hertz (Hz), of the transformer.

Primary (zigzag) nominal voltage Vp: The phase-to-phase nominal voltage in volts RMS, for the primary winding of the transformer.

Secondary nom. voltage phase shift: The phase-to-phase nominal voltage, in volts RMS, and the phase shift, in degrees, for the secondary winding of the transformer.

Winding 1 zig-zag [R1 L1]: The resistance and leakage inductance of the windings 1 of the single-phase transformers used to implement the primary winding of the Zigzag Phase-Shifting Transformer.

Winding 2 zig-zag [R2 L2]: The resistance and leakage inductance of the windings 2 of the single-phase transformers used to implement the primary winding of the Zigzag Phase-Shifting Transformer.

Winding 3 secondary [R3 L3]: The resistance and leakage inductance of the windings 3 of the single-phase transformers used to implement the secondary winding of the Zigzag Phase-Shifting Transformer.

Magnetization resistance Rm: This parameter is accessible only if the Saturable core parameter on the Configuration tab is selected.

Saturation characteristic: The saturation characteristic for the saturable core. Specify a series of current/ flux pairs (in pu) starting with the pair (0,0).

NOTE: the ARTEMiS-Transformer with Switched Saturable Core only allow a two-segment saturation characteristic so only 3 pairs of points can be entered (including the (0,0) point).

Parameters (Y-D)

Units: Specify the units used (SI or PU) for Zigzag Phase-Shifting Transformer block. Two different blocks must be used for SI or PU units.

Nominal power and frequency: The nominal power rating, in volt-amperes (VA), and nominal frequency, in hertz (Hz), of the transformer.

Primary (Y) nominal voltage Vp: The phase-to-phase nominal voltage in volts RMS, for the primary winding of the transformer. This winding is always connected in Y.

Secondary nom. voltage: The phase-to-phase nominal voltage, in volts RMS, for the secondary winding of the transformer.

Secondary winding (abc) connection: the type of connection for the secondary windings. Available connection are: Y-Y, and Y-D (±30 deg.). Note that the winding neutral point connection is always available at both primary and secondary winding.

Winding 1 impedance [R1 L1]: The resistance and leakage inductance of the windings 1 of the single-phase transformers used to implement the primary winding of the Zigzag Phase-Shifting Transformer.

Winding 2 impedance [R2 L2]: The resistance and leakage inductance of the windings 2 of the single-phase transformers used to implement the primary winding of the Zigzag Phase-Shifting Transformer.

Magnetization resistance Rm: This parameter is accessible only if the Saturable core parameter on the Configuration tab is selected.

Saturation characteristic: The saturation characteristic for the saturable core. Specify a series of current/ flux pairs (in pu) starting with the pair (0,0).

NOTE: the ARTEMiS-Transformer with Switched Saturable Core only allow a two-segment saturation characteristic so only 3 pairs of points can be entered (including the (0,0) point).

Advanced Parameters

Use SPS injection method: Disable the Switching Core Saturation and use standard SPS injection method to simulate saturation

Disable saturation: Disable the Switched Core saturation (only if **Use SPS injection method** is not selected)

Unique Global Tag: Unique tag within the COMPLETE model to route some internal flux signalsinside the transformer model. If two ARTEMiS Switched Core transformer model with the same **Unique Global Tag** are in the same simulation model, an error will occur.

Examples

Example 1: Energization of a zig-zag transformer with an floating source

This example case makes the energization of a 3-phase zigzag-Y transformer on an inductive load. The load is has about 0.8 p.u. of active power 0.6 pu of reactive power. The transformer has an total impedance of 0.26 pu and is energized from rest with a balanced source of 1 pu of voltage.

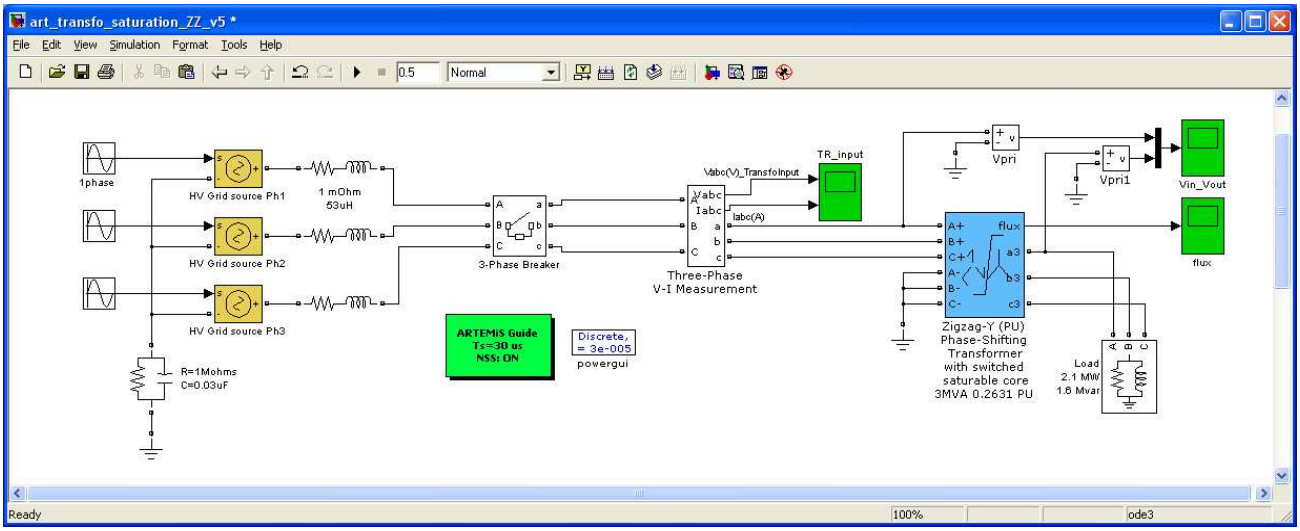


Figure 42:Test model for the zigzag-Y transformer

The saturation curve is depicted on the next figure.

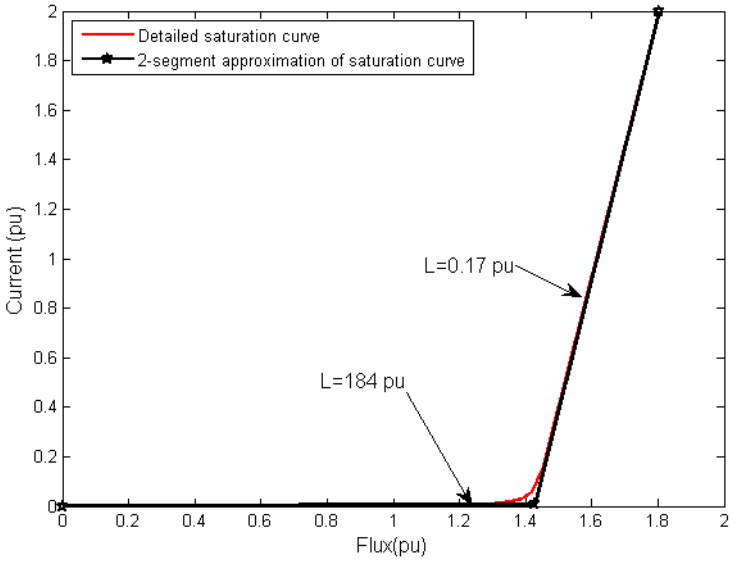


Figure 43:Saturation curve of the zigzag transformer of the test model

The particularity of this model is that it simply cannot be simulated in real-time with SimPowerSystems only. If one try to simulate this model with the current injection with delay method of SPS, the model is unstable, event at 0.1 µs!

With the ARTEMiS-Transformer with Switched Saturable Core, the model is stable and very accurate at time step of 30µs and more.

The following curves compare the simulation results of the model with ARTEMiS-Transformer with Switched Saturable Core at 30µs with one made with native SimPowerSystems at 1µs, with an algebraic loop. This means that the solver becomes iterative in this case and not suitable for real-time simulation anyway. It can however be taken for off-line simulation reference.

The simulations are conducted with positive and negative angle phase shifts to verify the internal connection of the ARTEMiS models.

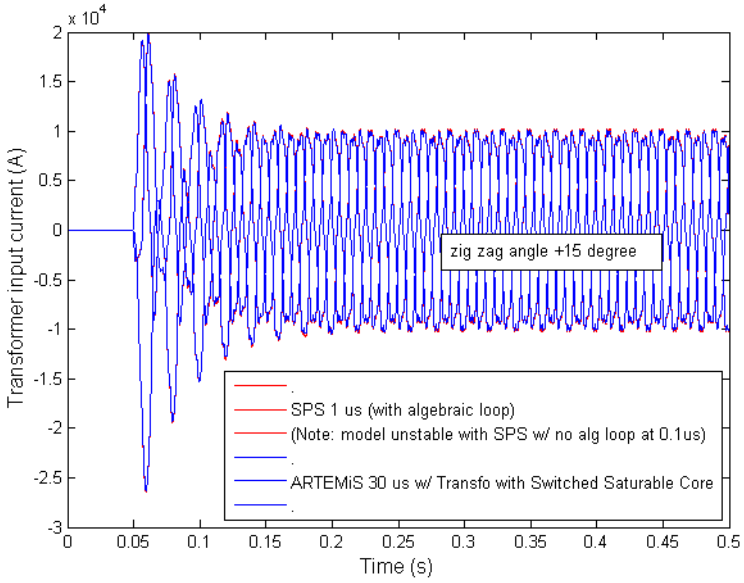

x 10^4
Transformer input current (A)
Time (s)
zig zag angle +15 degree
SPS 1 us (with algebraic loop)
(Note: model unstable with SPS w/ no alg loop at 0.1us)
ARTEMiS 30 us w/ Transfo with Switched Saturable Core

Figure 44:Zigzag transformer input current comparison (positive 15° phase shift)

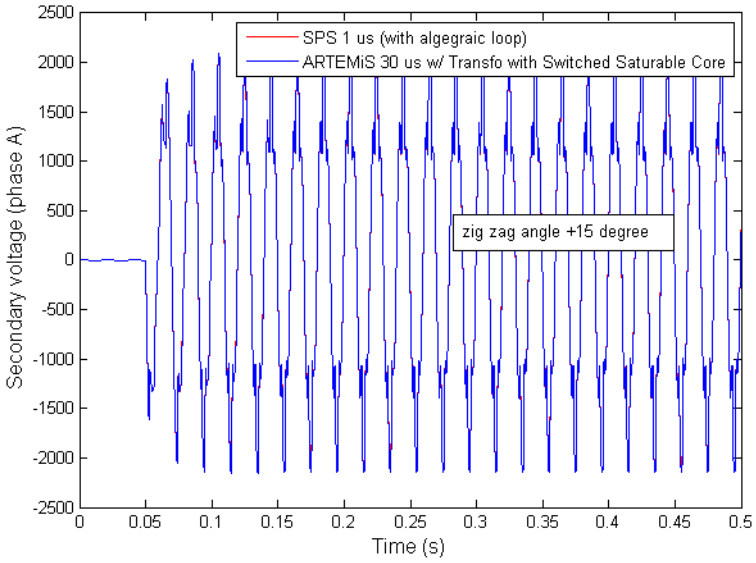

Secondary voltage (phase A)
Time (s)
SPS 1 us (with algegraic loop)
ARTEMiS 30 us w/ Transfo with Switched Saturable Core
zig zag angle +15 degree

Figure 45:Zigzag transformer output voltage comparison (positive 15° phase shift)

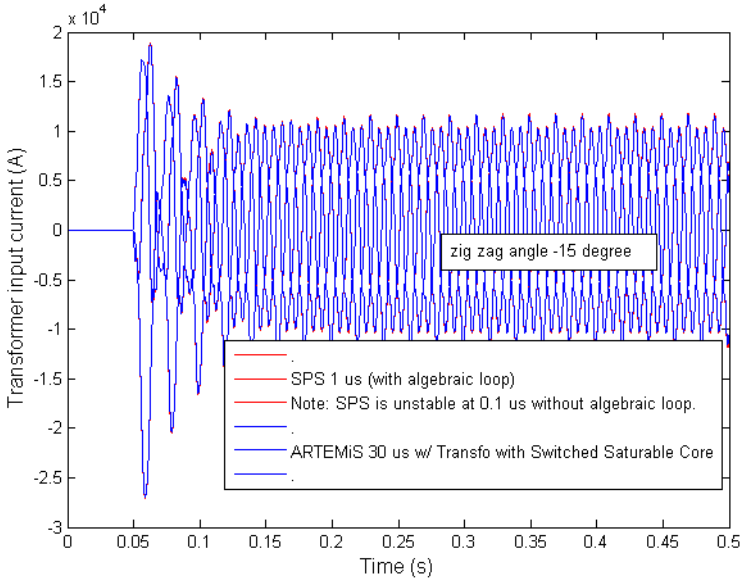

x 10^4
Transformer input current (A)
Time (s)
zig zag angle -15 degree
.
SPS 1 us (with algebraic loop)
Note: SPS is unstable at 0.1 us without algebraic loop.
.
ARTEMiS 30 us w/ Transfo with Switched Saturable Core
.

Figure 46:Zigzag transformer input current comparison (negative 15° phase shift)

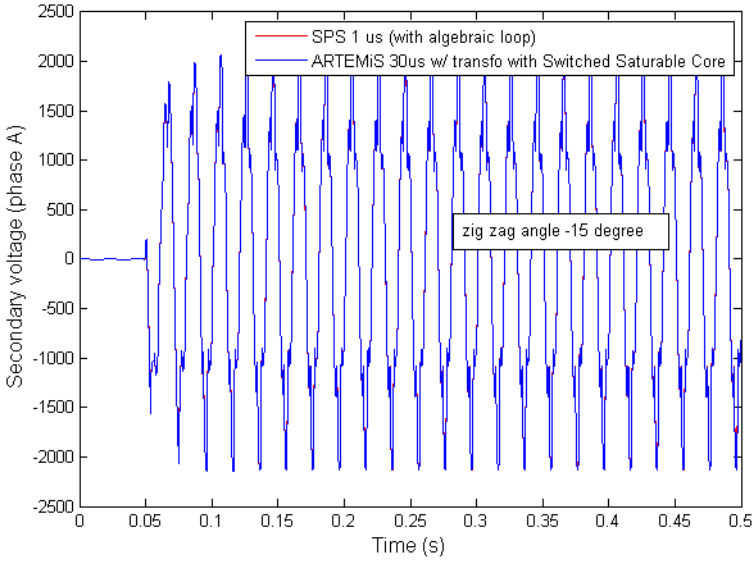

Secondary voltage (phase A)
Time (s)
SPS 1 us (with algebraic loop)
ARTEMiS 30us w/ transfo with Switched Saturable Core
zig zag angle -15 degree

Figure 47:Zigzag transformer output voltage comparison (negative 15° phase shift)

Input-Outputs

A+, B+, C+ (PM-type connectors): 1st winding of zigzag. Positive polarity zigzag winding connection.

A-, B-, C-: (PM-type connectors). 2nd winding of zigzag. Negative polarity zigzag winding connection.

a3, b3, c3: (PM-type connectors). 3rd (or secondary) winding connected in Y.

flux: core flux signals (size 3)

Characteristics and Limitations

1- The ARTEMiS-Transformer with Switched Saturable Core can only work with the ARTEMiS GUIde block present in the model. The first reason is that the ARTEMiS saturable transformer models are used to provide the core flux readings required by the model. The 2nd reason is that the damping properties of the ARTEMiS **art5** solver are required to obtain

Direct Feedthrough	N/A
Discrete sample time	Yes
RT-LAB XHP support	Yes
Work offline	Yes

Related Items

ARTEMIS Distributed Parameters Line, ARTEMiS Stubline, ARTEMiS-SSN Nodal interface Blocks, ARTEMiS-SSN Frequency Dependent Line.

Library

ARTEMiS (Advanced Real-Time ElectroMagnetic Simulator)

Block

The ARTEMiS-SSN Nodal interface Blocks are used to define nodes and groups of the ARTEMiS-SSN solver. The SSN (State-Space Nodal) solver is a simulation solver that use nodal method to couple together, without delays, groups defined by their discretized SPS state-space equation or any model that has a discrete resistive companion model compatible with the nodal method of EMTP.

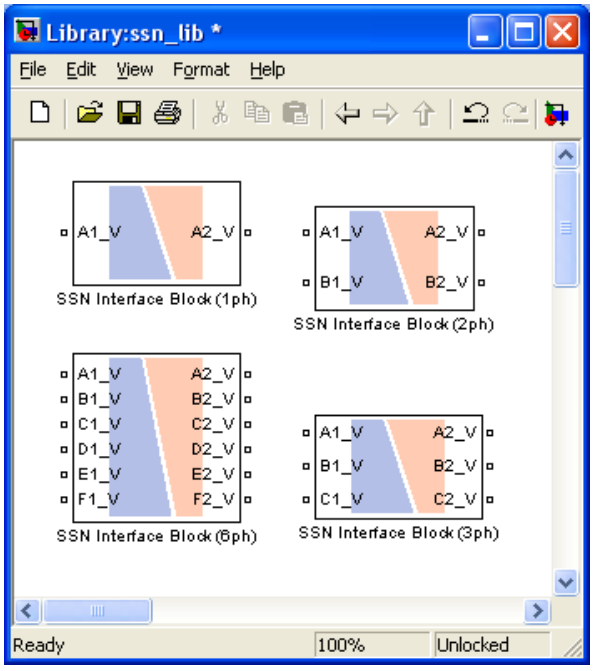


Figure 48:ARTEMiS-SSN Nodal interface Blocks

Mask

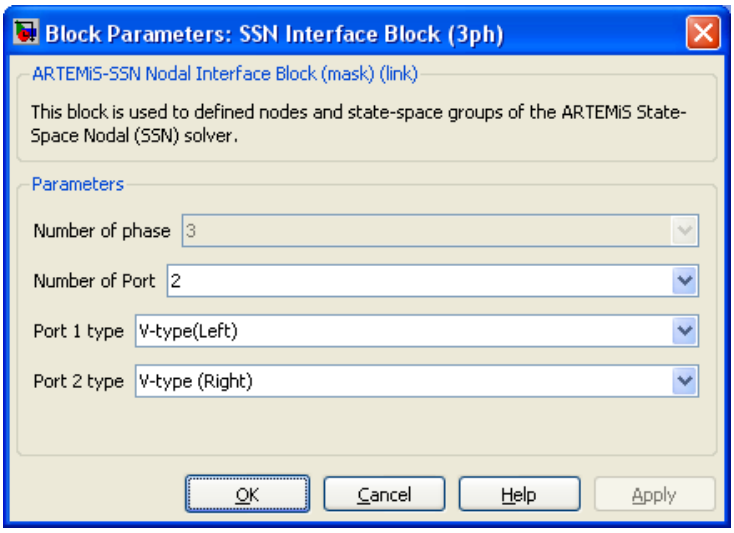


Figure 49:Mask of the ARTEMiS-SSN Nodal Interface Blocks (3-phase case)

Description

The ARTEMiS-SSN Nodal Interface Blocks (NIB)is used to define nodal point and state-space groups in a SimPowerSystems schematic within the ARTEMiS-SSN solver. Each block instance defines a node by itself. The NIB also defines the perimeter of the SSN groups.

Parameters

Number of phase: Set the number of phase for the NIB.

Number of Ports: Set the number of Ports of the block. All phase of a single port connects to a single SSN group.

Port *x* type: The ***Number of Ports*** parameter sets the number of ***Port x type*** (where x= 1 to 16) accesible by the user. For each ***Port x type*** parameter, 6 different options are possible.

V-type(Left) : Voltage type interface to the state-space groups, with ports on the left side

V-type (Right): Voltage type interface to the state-space groups, with ports on the right side

I-type(Left): Current type interface to the state-space groups, with ports on the left side

I-type(Right): Current type interface to the state-space groups, with ports on the right side

X-type(Left): External SSN group type interface, with ports on the left side

X-type(Right): External SSN group type interface, with ports on the right side

These various options are used to connect different types of SSN groups:

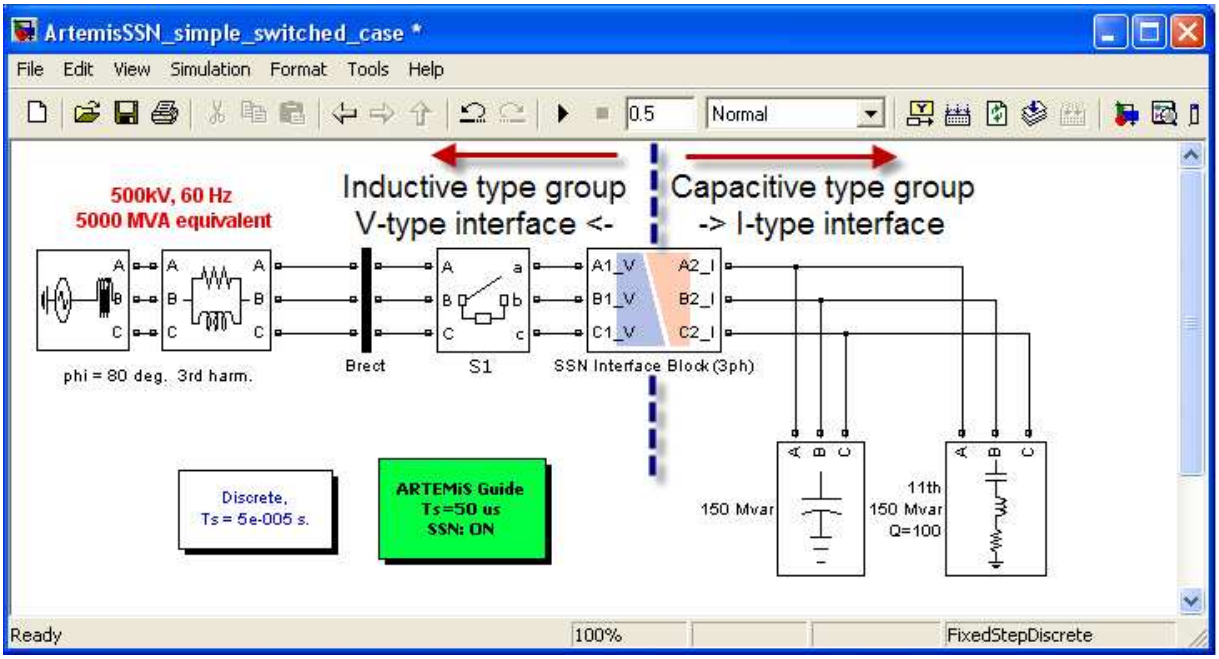
- Inductive type SSN groups require a V-type interface
- Capacitive type SSN groups require a I-type interface
- External SSN model, such as the FD-line model, require a X-type interface

Some example will be given to explain this

Examples

Example 1: NIB with I-type and V-type interface

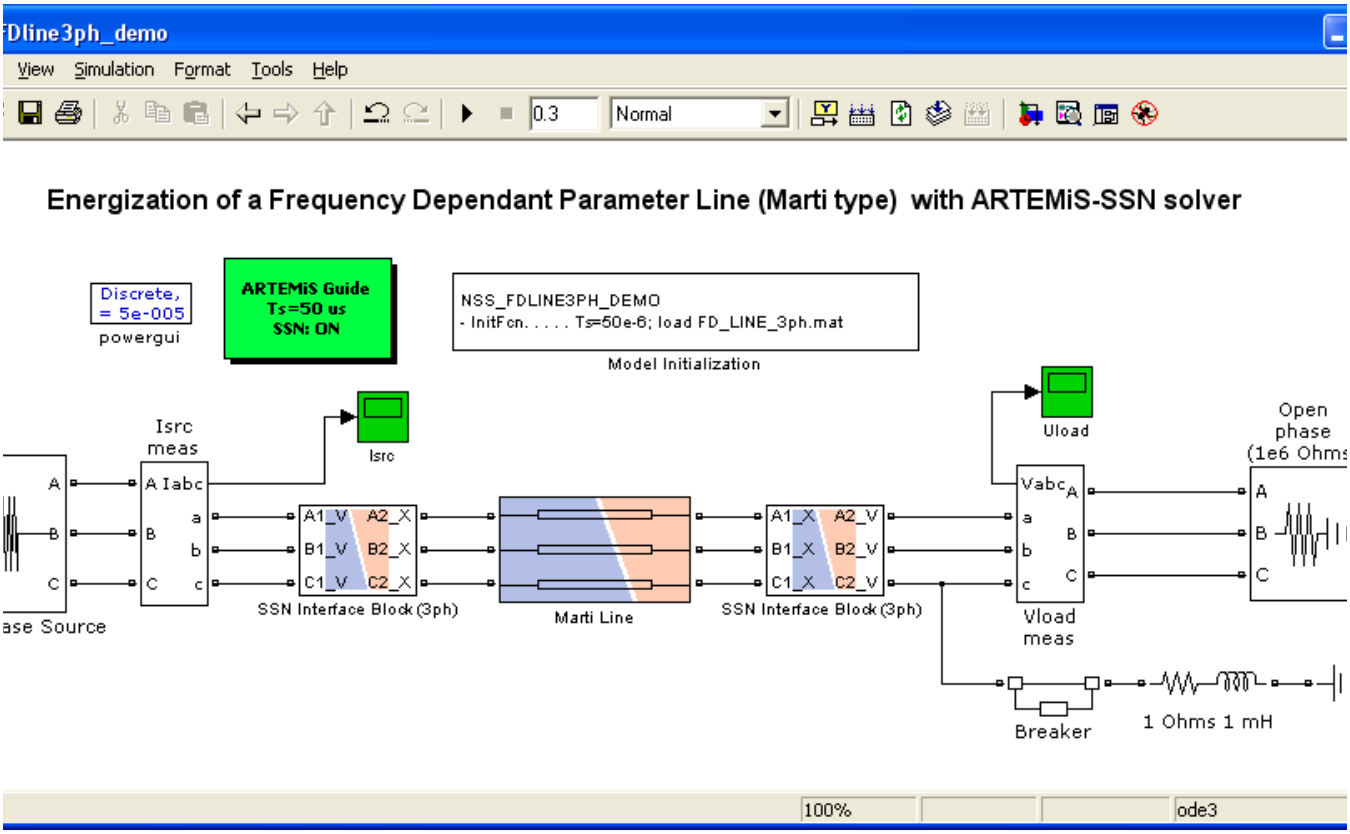
Take the following model, ArtemisSSN_simple_switched_case.mdl, which contains a switched inductive source connected to a filter bank.



The model has been separated into 2 SSN groups, with the intersection being defined by the NIB. The NIB interface is I-type in the direction of the capacitor of the filter bank while it is V-type in the direction of the inductive source. The type of interface is displayed on the block. The NIB also defines the 3 node that will used internally in the nodal part of the SSN solution.

Example 2: NIB with X-type interface, for SSN external models

The model below simulates a Frequency Dependent Parameter Transmission Line (FD-line) based on the model originally developped by Marti. This FD-line model is internally coded using the nodal approach and can only produce discrete resistive companion model data like the model discrete admittance and history current sources. The direct inclusion of the line characteristic impedance Zc(ω) into a state-space method would have produce huge ABCD matrices becaue of the many states that compose Zc(ω).



For this reason, the SSN approach is prefered when the interface of this type of model to the state-space method of SimPowerSystems. To make the interface, the NIB block must have the type-X chosen and connected toward the external SSN model, an FD-line model in this case. AS previously, the NIB also defines the nodal point of the SSN solution. In this case, 6 nodes will be used in the nodal solution part of SSN.

Input-Outputs

PM-type connectors

Characteristics and Limitations

V- and I-type NIB blocks are used to compute state-space equation of the SSN groups, and are internally composed of current or voltage sources. State-space equation causality restrictions apply to these blocks. This is why V-type (internal voltage source) connects to inductive groups and I-type (internal current source) to capacitive type groups.

Direct Feedthrough	N/A
Discrete sample time	Yes
RT-LAB XHP support	Yes
Work offline	Yes

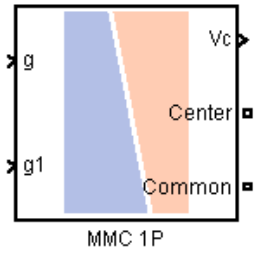
Related Items

ARTEMIS Distributed Parameters Line, ARTEMiS Stubline, ARTEMiS-SSN Frequency Dependent Line.

Library

ARTEMiS (Advanced Real-Time ElectroMagnetic Simulator)

Block



Mask

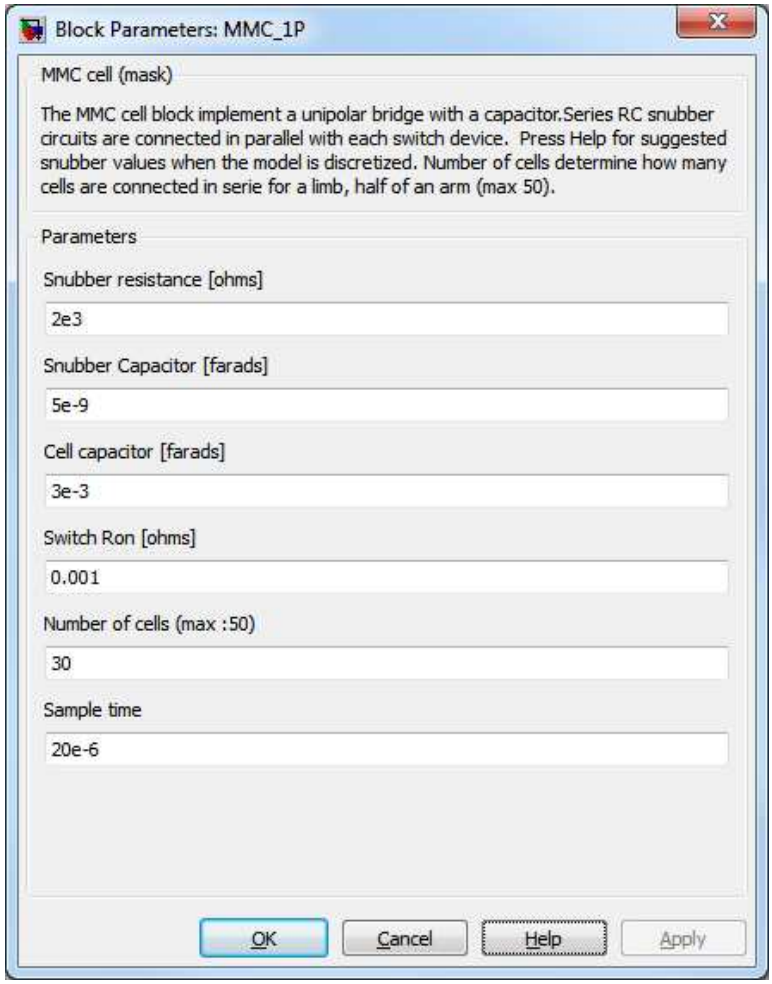

Block Parameters: MMC_1P
MMC cell (mask)
The MMC cell block implement a unipolar bridge with a capacitor.Series RC snubber circuits are connected in parallel with each switch device. Press Help for suggested snubber values when the model is discretized. Number of cells determine how many cells are connected in serie for a limb, half of an arm (max 50).
Parameters
Snubber resistance [ohms]
2e3
Snubber Capacitor [farads]
5e-9
Cell capacitor [farads]
3e-3
Switch Ron [ohms]
0.001
Number of cells (max :50)
30
Sample time
20e-6
OK
Cancel
Help
Apply

Figure 50:Mask of MMC 1P block

Description

The MMC cell block implement a unipolar bridge with a capacitor. Series RC snubber circuits are connected in parallel with each switch device. Press Help for suggested snubber values when the model is discretized. The gates are controlled by Double signals. The following figure presents the equivalent electrical circuit of the MMC cell block implement a unipolar bridge.

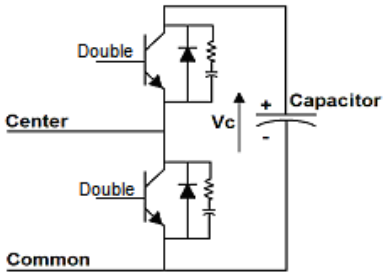


Figure 51:Equivalent Electrical Circuit of the MMC cell Block

When the upper switch or upper anti-parallel diode conducts, voltage between the Center and the Common equals Vc (minus internal voltage drops). When the lower switch or diode of the leg conducts, this voltage is equal to 0 (plus internal voltage drops).

The RC snubber in shunt with the switch are required to solve numerical oscillation. Using the time step and the equivalent inductance of the circuit the value of the Rsnubber and Csnubber are given by the following equation

$$R_{Snubber} = \frac{\pi}{Ts \cdot 5} \cdot L_{eq} \cdot \frac{1}{nbcells}$$

$$C_{Snubber} = \frac{1}{\left(L_{eq} \cdot \frac{2 \cdot \pi}{Ts \cdot 15}\right)^2} \cdot nbcells$$

Where nbcells is the number of cells in series and Leq is the equivalent inductance

Parameters

Snubber resistance: Snubber resistance value, only used in high impedance mode.

Snubber Capacitor: Snubber capacitor value, only used in high impedance mode.

Cell capacitor: Value of the cell's capacitor .

Ron: Internal resistance of the selected device, in ohms.

Number of cells: This determine how many cells are connected in series. A maximum of 50 cells can be connected in series. If more then 50 cells are required, a second MMC_1P block need to be connected in series.

Sample time: Time at which the capacitor voltage will be computed.

Inputs

g1 (double): double signals that controlled the upper switch gates. This signal has to be a vector of same length then the number of cells. A signal value of 1 indicates the switch is conducting, while a value of zero indicates the switch is OFF.

g2 (double): double signals that controlled the lower switch gates. This signal has to be a vector of same length then the number of cells. A signal value of 1 indicates the switch is conducting, while a value of zero indicates the switch is OFF.

Center (SPS): Middle point of the cell.

Common (SPS): Common point of the cell.

Outputs

Vc (double): The voltage at the cell's capacitor, vector of same length then the number of cells

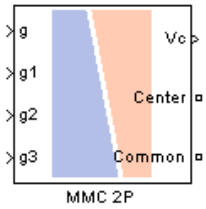
Characteristics

Direct Feedthrough	No
Sample time	Parameter
Work offline	Yes
Dimensionalized	Yes

Library

ARTEMiS (Advanced Real-Time ElectroMagnetic Simulator)

Block



Mask

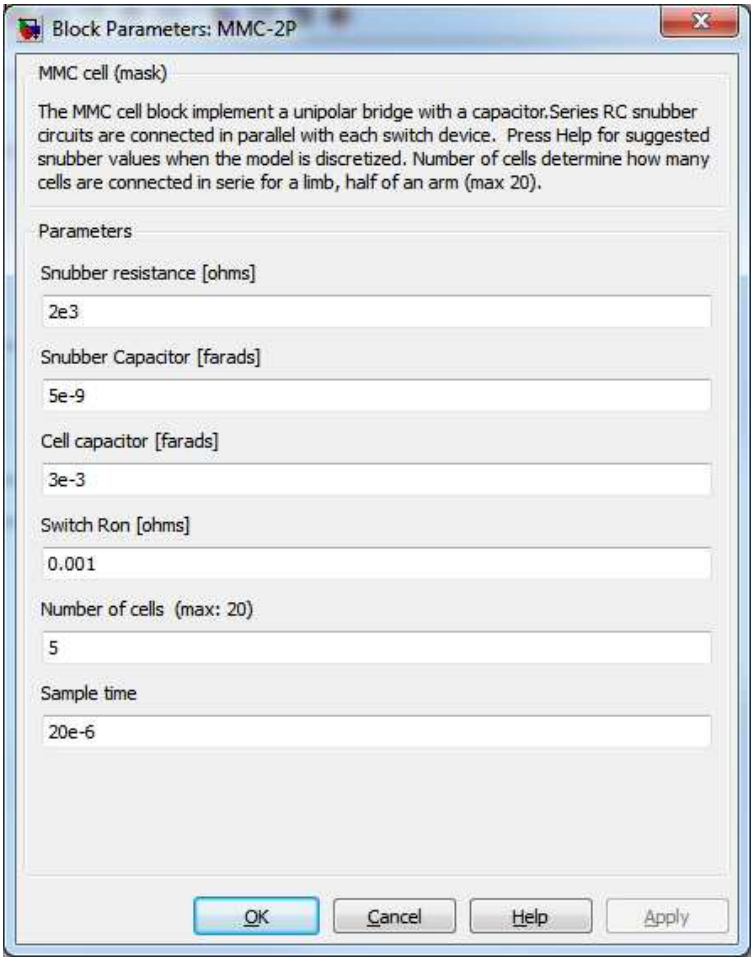

Block Parameters: MMC-2P
MMC cell (mask)
The MMC cell block implement a unipolar bridge with a capacitor.Series RC snubber circuits are connected in parallel with each switch device. Press Help for suggested snubber values when the model is discretized. Number of cells determine how many cells are connected in serie for a limb, half of an arm (max 20).
Parameters
Snubber resistance [ohms]
2e3
Snubber Capacitor [farads]
5e-9
Cell capacitor [farads]
3e-3
Switch Ron [ohms]
0.001
Number of cells (max: 20)
5
Sample time
20e-6
OK
Cancel
Help
Apply

Figure 52:Mask of MMC 2P block

Description

The MMC-2P cell block implement a bipolar bridge with a capacitor. Series RC snubber circuits are connected in parallel with each switch device. Press Help for suggested snubber values when the model is discretized. The gates are controlled by Double signals. The following figure presents the equivalent electrical circuit of the MMC cell block implement a unipolar bridge.

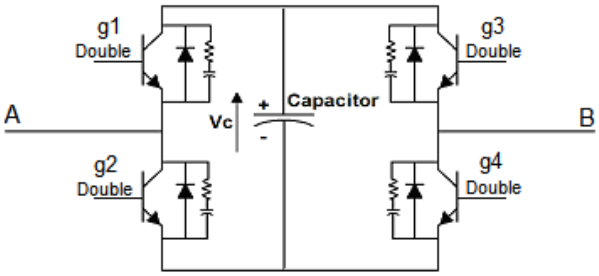


Figure 53:Equivalent Electrical Circuit of the MMC-2P cell Block

The voltage between A and B is determined by the switching applied to g1 to g4. g1 and g2 must be complementary and so does g3 and g4.

The RC snubber in shunt with the switch are required to solve numerical oscillation. Using the time step and the equivalent inductance of the circuit the value of the Rsnubber and Csnubber are given by the following equation

$$R_{Snubber} = \frac{\pi}{Ts \cdot 5} \cdot L_{eq} \cdot \frac{1}{nbcells}$$

$$C_{Snubber} = \frac{1}{\left(L_{eq} \cdot \frac{2 \cdot \pi}{Ts \cdot 15}\right)^2} \cdot nbcells$$

Where nbcells is the number of cells in series and Leq is the equivalent inductance

Parameters

Snubber resistance: Snubber resistance value, only used in high impedance mode.

Snubber Capacitor: Snubber capacitor value, only used in high impedance mode.

Cell capacitor: Value of the cell's capacitor .

Ron: Internal resistance of the selected device, in ohms.

Number of cells: This determine how many cells are connected in series. A maximum of 20 cells can be connected in series. If more then 20 cells are required, a second MMC_2P block need to be connected in series.

Sample time: Time at which the capacitor voltage will be computed.

Inputs

g1 (double): double signals that controlled the upper left switch gates. This signal has to be a vector of same length then the number of cells. A signal value of 1 indicates the switch is conducting, while a value of zero indicates the switch is OFF.

g2 (double): double signals that controlled the lower left switch gates. This signal has to be a vector of same length then the number of cells. A signal value of 1 indicates the switch is conducting, while a value of zero indicates the switch is OFF.

g3 (double): double signals that controlled the upper right switch gates. This signal has to be a vector of same length then the number of cells. A signal value of 1 indicates the switch is conducting, while a value of zero indicates the switch is OFF.

g4 (double): double signals that controlled the lower right switch gates. This signal has to be a vector of same length then the number of cells. A signal value of 1 indicates the switch is conducting, while a value of zero indicates the switch is OFF.

A (SPS): Middle left point of the cell.

B (SPS): Middle right point of the cell.

Outputs

Vc (double): The voltage at the cell's capacitor, vector of same length then the number of cells

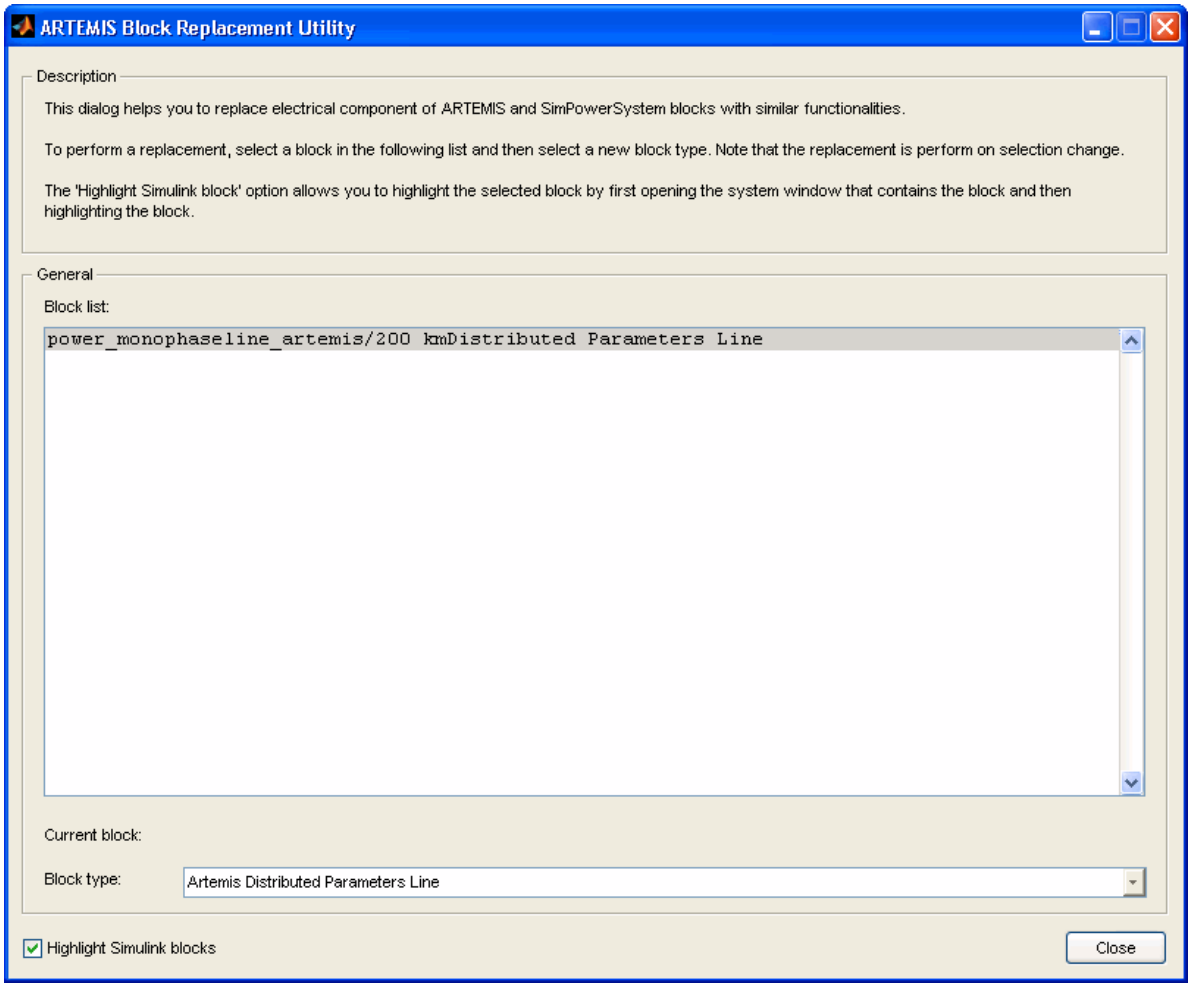
Characteristics

Direct Feedthrough	No
Sample time	Parameter
Work offline	Yes
Dimensionalized	Yes

Description

This function helps replacing SimPowerSystems electrical blocks by ARTEMIS electrical blocks or replacing ARTEMIS electrical blocks by SimPowerSystems electrical blocks. This function is useful because ARTEMIS provides advanced blocks for real-time simulation; these blocks contain an optimized implementation of the SPS mathematical model which make them better suited for real-time simulation.

This function also provides an optional interface to help the user select the blocks to be replaced. The figure below shows the dialog that appear when the function is called with the default argument.


ARTEMIS Block Replacement Utility
Description
This dialog helps you to replace electrical component of ARTEMIS and SimPowerSystem blocks with similar functionalities.
To perform a replacement, select a block in the following list and then select a new block type. Note that the replacement is perform on selection change.
The 'Highlight Simulink block' option allows you to highlight the selected block by first opening the system window that contains the block and then highlighting the block.
General
Block list:
power_monophaseline_artemis/200 kmDistributed Parameters Line
Current block:
Block type:
Artemis Distributed Parameters Line
Highlight Simulink blocks
Close

Note that ARTEMIS currently only supports the Distributed Parameters line block. Other decoupling blocks than the Distributed Parameters line will be supported in a future release.

Usage

opReplaceSpsBlocks(modelName, operation, searchDepth);

Inputs

modelName	Name of the model to modify.
operation	Optional argument that specified the type of operation to perform when replacing the blocks. 1- ReplaceBlocks: open a dialog that will help to switch between the real-time ARTEMIS blocks and the non-real-time SPS blocks. 2- ReplaceSpsBlocks: automatically replace all SPS blocks by their real-time ARTEMIS equivalent, 3- ReplaceArtemisBlocks: automatically replace all ARTEMIS blocks by their non real-time SPS equivalent. The default value is “ReplaceBlocks”.
searchDepth	Optional integer that constrains the model search to a specific depth.

Outputs

None

Example

To open a dialog that will help to switch between the real-time ARTEMIS blocks and the non-real-time SPS blocks:
opReplaceSpsBlocks(modelName);

To automatically replace all SPS blocks by their real-time ARTEMIS equivalent:
opReplaceSpsBlocks(modelName, 'ReplaceSpsBlocks');

To automatically replace all ARTEMIS blocks by their non real-time SPS equivalent:
opReplaceSpsBlocks(modelName, 'ReplaceArtemisBlocks')

Related Items

ARTEMIS Distributed Parameters Line, **ARTEMiS Guide**

Known limitations (ARTEMiS v6.0 release)

6

The following issues and limitations of ARTEMIS v5.2 are known to Opal-RT.

ARTEMiS limitations

1- 3-level bridge with ’ideal switch’ option not supported in ARTEMIS-DTCSE mode.

2- Maximum number of switch is 28 in a single topologicaly connected network for all mode even Dynamic calculation

3- Stubline usage causes instability when using ARTEMIS-DTCSE mode.

4- ARTEMIS distributed parameters line have no 'Measurements' options. SPS mesurement blocks are an alternative for line measurements.

5- ARTEMIS distributed parameters lines are not initialized with stady state currents and voltages. This can results in some transients at the beginning of the simulation.

6- The trapezoidal solver does not support RT-Events based switch gating signals

7- Circuit containing SPS Multimeter blocks are simulated into a single state-space system.

SimPowerSystems 4.6- 5.0 limitations

SPS Neutral blocks: There is a limitation in SimPowerSystems (v4.6 and v5.0) that prevent the effective separation (or decoupling) of independant systems of state-space equation if any SPS Neutral block is present in the model. This does not affects the simulation accuracy of models but only slows them down because big matrix systems are formed. In RT applications, this will increased the required memory and probably increase the minimal sample time. The effect is similar to the ***Ground Connections*** problem described next.

Ground Connections: There is currently a bug in SPS 4.6 (R2008a) with regards to separation/decoupling of state-space systems.

If , for example, 3 components are wired together to a single SPS 'Ground', the 3 componants will be put in the same state-space system.

If the same componants are connected to 3 distinct SPS 'Ground' blocks, then the 3 componants will be put into 3 differents state-space systems (provided that there is no other connections between the components)

Electrically speaking, the 2 cases are identical but it affect the capacity of separation. The user is advised to verify the effective subsystems separation as it appears at the MATLAB prompt at the beginning of the simulation with ARTEMiS. The following prompt output shows that the power_x model is separated into 2 subsystems:

```
SimPowerSystems processing circuit #1 of power_x ...
Computing state-space representation of linear electrical circuit ...
 (13 states ; 9 inputs ; 8 outputs ; 3 switches)
...
ARTEMIS: approx. memory required for full matrix precomputation: 0.037056 Mb
Ready.
```

```
Third-Party Rule block detected: power_transfosat/ARTEMIS Guide
SimPowerSystems processing circuit #2 of power_x ...
Computing state-space representation of linear electrical circuit ...
 (13 states ; 9 inputs ; 8 outputs ; 3 switches)
...
ARTEMIS: approx. memory required for full matrix precomputation: 0.037056 Mb
Ready.
```